Contribution (Invited)

Micro and Nanofabrication for Graphene Electronics

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Relevant examples of synthesis and device fabrication technology applied to graphene materials will be presented. Special attention will be devoted to the application of micro and nanopatterning techniques to obtain graphene based electronic devices. At the IMB-CNM, an integral approach on graphene technology is currently implemented.

For instance, optimization of the processing of epitaxial graphene on SiC (EG-SiC) is applied to all available synthetic materials, i.e. in the form of 1) full coverage [1], 2) isolated flakes [2] and 3) selectively grown [3] graphene materials. Additionally, their combination with both conventional and unconventional planar technology techniques include device fabrication methods such as, respectively, ion implantation for gating and local anodic oxidation by atomic force microscope for device resistance tuning [4].

Apart from conventional synthesis by chemical vapor deposition (CVD) on Cu, up to 4" wafer scale, other examples of micro-nanostructured graphene materials which could be presented are the use of plasma enhanced CVD for the synthesis of porous vertically oriented graphene sheets. These so-called carbon nanowalls have been applied as electrode materials for supercapacitor devices [5] and Li-ion batteries [6]. Alternatively, original methods such as thermal graphitization of ultrathin diamond-like carbon membranes patterned by focused ion beam induced deposition could be also introduced [7].

Additional works on processing such as delamination and transfer techniques as well as integration of transistors, both at wafer scale, based on CVD graphene, for biomedical applications, or single wall carbon nanotubes [8], for chemical sensing, can be shown. These are examples of the capability for batch fabrication of micro-nanoelectronic devices and systems.

Finally, other examples of innovative nanofabrication strategies and nanoelectronic applications of 2D materials, such as applying block copolymer (BCP) masks to graphene (Fig. 1), for its quantum confined electronic performance, and graphene oxide (GO), for RRAM devices (Fig. 2), are some of the most recent investigations under development at the IMB-CNM.

References

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Figures

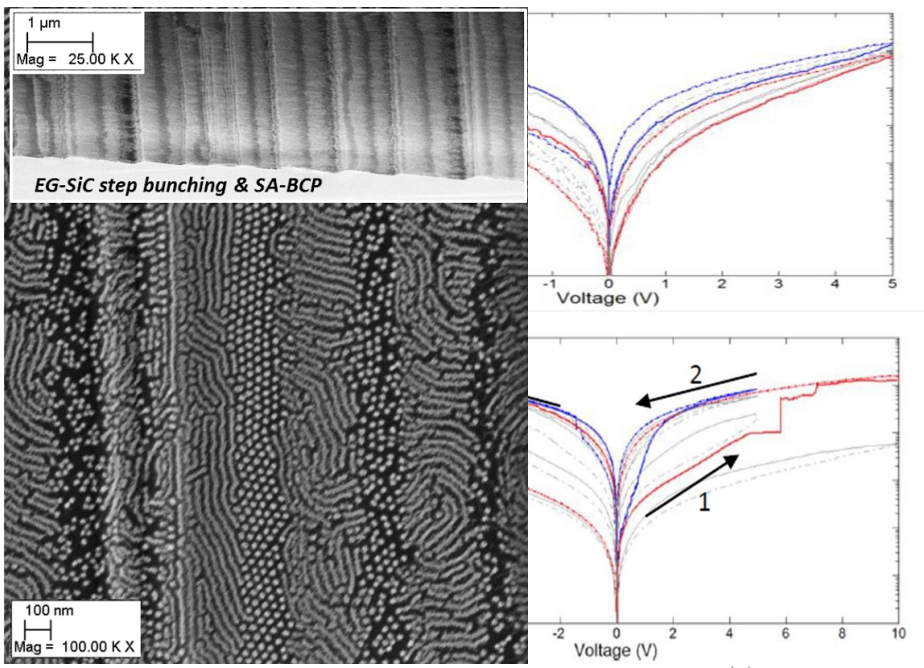

Figure 1: LEFT: Top view SEM image of thermally annealed 2L0 thick Nanostrength EO® C35 PS-b-PMMA on Si-face EG-SiC after sequential infiltration synthesis plus plasma O_2, for high contrast directed self-assembly BCP observation; e.g. of a characteristic closely-packed (ordered) array of dots (center stripe). Top inset is a cross section of the same sample, to show the typical step bunching of EG-SiC and formation of terrace suprastructured stripes. Figure 2: RIGHT: I/V curves of MIM devices with ten GO deposition cycles. The diversity of observed resistive switching behaviours suggests that efficient GO film should be thicker and grain size more uniform to provide a more robust operation.