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Silicon- and Graphene-based FETs for THz technology

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A mi familia
con cariño

Abstract

Silicon- and Graphene-based FETs for THz technology

This Thesis focuses on the study of the response to Terahertz (THz) electromagnetic radiation of different silicon substrate-compatible FETs. Strained-Si MODFETs, state-of-the-art FinFETs and graphene-FETs were studied.
The first part of this thesis is devoted to present the results of an experimental and theoretical study of strained-Si MODFETs. These transistors are built by epitaxy of relaxed-SiGe on a conventional Si wafer to permit the fabrication of a strained-Si electron channel to obtain a high-mobility electron gas. Room temperature detection under excitation of 0.15 and 0.3 THz as well as sensitivity to the polarization of incoming radiations were demonstrated. A two-dimensional hydrodynamic-model was developed to conduct TCAD simulations to understand and predict the response of the transistors. Both experimental data and TCAD results were in good agreement demonstrating both the potential of TCAD as a tool for the design of future new THz devices and the excellent performance of strained-Si MODFETs as THz detectors (75 V/W and 0.06 nW/Hz$^{0.5}$).
The second part of the Thesis reports on an experimental study on the THz behavior of modern silicon FinFETs at room temperature. Silicon FinFETs were characterized in the frequency range 0.14-0.44 THz. The results obtained in this study show the potential of these devices as THz detectors in terms of their excellent Responsivity and NEP figures (0.66 kV/W and 0.05 nW/Hz$^{0.5}$).
Finally, a large part of the Thesis is devoted to the fabrication and characterization of Graphene-based FETs. A novel transfer technique and an in-house-developed setup were implemented in the Nanotechnology Clean Room of the USAL and described in detail in this Thesis. The newly developed transfer technique enables to encapsulate a graphene layer between two flakes of h-BN. Raman measurements confirmed the quality of the fabricated graphene heterostructures and, thus, the excellent properties of encapsulated graphene. The asymmetric dual grating gate graphene FET (ADGG-GFET) concept was introduced as an efficient way to improve the graphene response to THz radiation. High quality ADGG-GFETs were fabricated and characterized under THz radiation. DC measurements confirmed the high quality of graphene heterostructures as it was shown on Raman measurements. A clear THz detection was found for both 0.15 THz and 0.3 THz at 4K when the device was voltage biased either using the back or the top gate of the G-FET. Room temperature THz detection was demonstrated at 0.3 THz using the ADGG-GFET. The device shows a Responsivity and NEP around 2.2 mA/W and 0.04 nW/Hz$^{0.5}$ respectively at respectively at 4K.
It was demonstrated the practical use of the studied devices for inspection of hidden objects by using the in-house developed THz imaging system.

Key words: THz, Plasma-waves, FETs, MODFETs, FinFETs, Silicon, Graphene.

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.

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Introduction and motivation

Terahertz (THz) rays are located in the spectral region between the microwave and the infrared portions of the electromagnetic spectrum (Fig. 0.1). While there is no a unique definition of the THz range, it is generally defined as the part of the EM spectrum from 0.1 to 10 THz, having respectively wavelengths from 3 mm down to 30 μm (Figure 0.1). It covers the upper part of the millimeter waves spectral range (30-300 GHz), the whole range of submillimeter waves (0.3 to 3 THz) and the lower end part of the infrared range (3 to 10 THz).

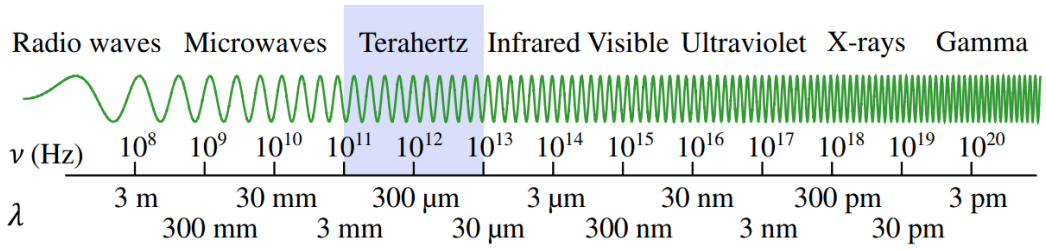


Figure 0.1 THz range location on the Electromagnetic spectrum [1]

The THz region remains one of the most understudied range in the EM spectrum even though its potential applications in sensing, security, spectroscopy and communication are of big interest. The attractive features of THz radiation for applications are: (i) most packaging materials (such as paper or plastics) and cloths are transparent to this radiation [2] (ii) Many substances have "fingerprint" spectra in the THz range (iii) Due to its low photon energy (about one million times lower than the one of X-rays), THz radiation is non-ionizing and therefore not dangerous for human beings. The scientific interest in this field began in 1920 [3] and the term *terahertz* was first given by Fleming [4] in 1974. One of the first experiments on spectral content in the submillimeter range of interstellar medium was carried out by T.G. Philips and J. Keene in 1992 [5]. In the last decades a big interest was given to the development of terahertz devices for detection, emission, and mixing for different applications like: astronomy [6], spectroscopy (rotational, vibrational, and translational modes in the THz range are specific to a particular substance allowing to obtain a THz fingerprint) [7], [8], highly accurate thickness measurements of multi-layered materials [9], communications with a bandwidth significantly higher than those based on microwaves [10], nondestructive inspection based on both imaging of concealed objects and spectroscopy [11], metrology [12], quality control [13], among others. THz rays (T-rays) permit imaging with a diffraction-limited resolution similar to that of the human eye [14], and, since common optically opaque packaging materials are transparent to T-rays, the inspection of concealed objects is possible. More interesting applications related to THz technology was reported in references [15], [16].

THz region is also known as “THz GAP” (Figure 0.2) since neither optical nor microwave devices could fully conquer this domain [17]. Then, an emphasis on the development of THz systems is needed. Although THz sensors and emitters have been significantly developed in the last decade, most of them are bulky and

expensive, which limits their application and availability and, therefore, there is a long way ahead on the development of THz devices.

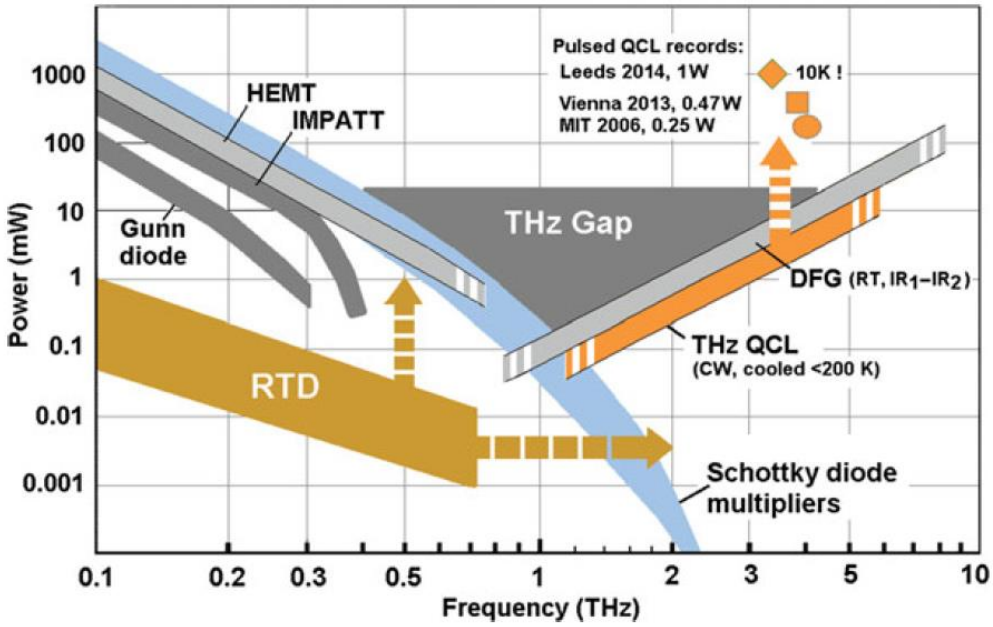


Figure 0.2 Map of available compact terahertz sources. The "THz gap" indicates the central frequency interval in which is hard to generate any larger radiation power. (Abbreviations: QCL Quantum Cascade Laser, DFG Difference Frequency Generation, RTD Resonant Tunneling Diode, HEMT High Electron Mobility Transistor, IMPATT IMPact ionization Avalanche Transit Time diode, CW Continuous Wave, RT Room Temperature) [17]

One of the most promising ways to emit and/or detect THz is based on the oscillations of plasma wave in the channel of submicron Field Effect Transistors (FETs) as proposed theoretically by Dyakonov and Shur in 1993 [18] - [19]. Nevertheless, only FETs entirely implemented in silicon CMOS process technology keep all the advantages of cost-effectiveness, scalability, high yield and high reliability. Therefore, silicon-based FETs or, at least, silicon substrate compatible technologies are potential candidates to develop efficient and cheap THz devices that operate at room temperature.

Since the first obtention of graphene flakes in 2004 [20], their excellent electronic and optical properties attracted interest to further investigate and develop room temperature graphene devices operating in the THz range that may contribute to close the THz GAP [21]. Moreover, new promising 2D materials also attract the interest to develop room-temperature THz devices. Nevertheless, it is well known that silicon dioxide (SiO_2), the most common substrate material for graphene, limits the performance of graphene devices and obscures its performance. Recently, dielectric hexagonal boron nitride (h-BN) emerged as the ideal substrate for graphene because both materials share of the same type of lattice. Graphene is transferred on an h-BN flake to fabricate graphene based vertical heterostructures showing better properties than the conventional graphene on SiO_2. One of the key advantages of 2D

materials and heterostructures is that they can be transferred to any substrate and therefore enables its integration in silicon integrated circuits.

In this Thesis, I focused my investigation line on the fabrication and characterization of different types of FETs (Si-based FET and Grpahene-based FETs) as THz detectors. This thesis manuscript was organized in four chapters as follow:

- Chapter 1 introduces the main mechanism of terahertz detection based on plasma-wave oscillations in the 2D channel of a FET. The theoretical model proposed by Dyakonov and Shur demonstrating that nanometric FETs can detect and emit THz radiation at frequencies above their cut-off frequency (f_t), is recalled.

- Chapter 2 is dedicated to describe the experimental setups and equipment used for the fabrication of graphene-based FETs and the characterization of the transistors studied across this PhD work. An in-house e system developed in the PhD was used to transfer the graphene and h-BN flakes. Devices were characterized electrically on wafer using a probestation and/or wire bonded using gold wires to conduct further electrical measurements. Characterization was conducted both at room and at low (down to 4K) temperatures. THz characterizations at 0.15 & 0.3 THz were performed at room temperature using an original dual-use THz imaging system. THz low temperature measurements were also conducted. More experiments on detection at higher terahertz frequency and on emission of THz radiation were performed in collaboration with CEZAMAT (Warsaw, Poland) and RIEC, (Tohoku University, Japan).

- Chapter 3: Two Si-based devices (Si-MODFET and FINFET) were experimentally studied in DC and as terahertz detectors. Strained-Si MODFETs were experimentally and theoretically characterized at 0.15 and 0.3 THz. A technology computer-aided design (TCAD) analysis based on a two-dimensional hydrodynamic model (HDM) was used to investigate the transistor response under THz radiation excitation. TCAD simulations were validated through comparison with experimental measurements carried at the THz Lab of USAL showing the potential of TCAD as a tool for the design of new THz devices. Moreover, both p-MOS and n-MOS silicon FinFETs were characterized on the THz range from 0.14 up to 0.44 THz at CEZAMAT laboratories (Warsaw, Poland). Both responsivity and Noise Equivalent Power (NEP) were extracted from measurement and show competitive values in comparison with other technologies. Terahertz imaging was performed to demonstrate the practical use of those devices for inspection applications.

- Chapter 4 is dedicated to graphene-based FETs. An Asymmetric-Dual-Grating-Gate Graphene-based FET (ADGG-GFET) was proposed, fabricated, abd characterized as THz detector. The device was fabricated using a graphene heterostructure where the graphene flake was sandwiched between two layers of h-BN and then processed to fabricate a FET using an artificial double-heterostructure (h-BN/graphene/h-BN) on a Si O_2/Si substrate. An experimental study from 4K up to room temperature was performed on the device as THz detector. Room temperature detection under 0.3 THz excitation was achieved and THz imaging was performed using the ADGG-GFET as the THz detector. Encouraging results using the ADGG-GFET for THz detection were obtained.

A conclusion of these works was presented at the final where all the obtained results were summarized. Moreover, as consequence of the promising results of the graphene-based devices, a future work plan will be presented as to continue the work of the presented thesis.

Chapter 1

Plasma-Wave oscillation in a FET & Terahertz detection

1.1 Analytic description

Dyakonov and Shur, first in 1993 [18] and later in 1996 [19], demonstrated theoretically the possibility of using submicron field-effect transistors (HEMTs, MOSFETs, …) as practical device operating in the terahertz range to build detectors, multipliers and mixers. They found that the oscilation frequency of plasma waves in the channel of a gated 2D system (Figure 1.1) is inversely propotional to the gate length. Hence, a gated 2D system (FET) with submicron gate length could operate at frequencies well above their cut-off frequency (f_t). When the electron plasma in the channel of a FET is excited by an external electromagnetic radiation, an AC electric field (U_{ac}) is induced and converted to a measurable DC voltage, between drain and source, via a nonlinear mechanism. These devices present many advantages: low cost, small size, room temperature operation, high time response, and tuning the frequency by the gate voltage as compared to other devices used in THz technology.

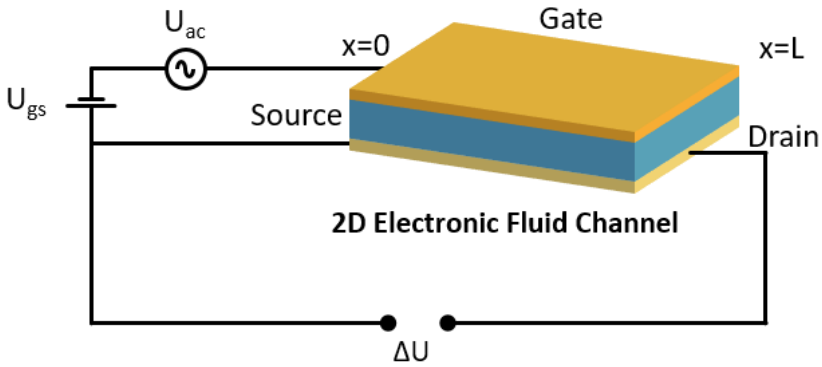


Figure 1.1 Schematic description of a FET operating as THz detector for an induced ac voltage

Figure 1.1 shows a schematic description of an ideal FET as a THz detector where a DC drain-to-source voltage (ΔU) appears as proportional to the incoming EM radiation. In an ideal case, the signal ΔU should show a resonant dependence on the incoming radiation with maxima at the plasma oscilation frequency, ω_0, and its odd harmonics $\omega_N = (1+2N)\omega_0$:

$$\omega_0 = \frac{\pi s}{2L} \tag{1.1}$$

where L is the transistor gate length and *s* is the plasma wave velocity that is given by the carriers' density and the gate-to-channel capacitance per unit area *C*:

$$s = \sqrt{\frac{e^2 n_s}{mC}} \tag{1.2}$$

e is the absolute value of the electron charge and m the electron mass. The carrier density in the FET channel is proportional to the gate swing or overdrive voltage (U_0) as:

$$n_s = \frac{CU_0}{e} \tag{1.3}$$

$U_0 = V_G - V_{th}$, V_G is the gate voltage and V_{th} the threshold voltage. Equation 1.3 only holds if the special variation of U(x) is larger than the gate-to-channel distance (gradual channel approximation). From those equations (1.1 to 1.3), an analytical expression can be obtained:

$$f_0 = \frac{1}{4}\sqrt{\frac{eU_0}{m}} \tag{1.4}$$

Figure 1.2 shows the resonance frequency versus U_0 for a GaAs based FET with a gate legth of 100 nm. It shows that submicron FET devices could operate as a THz detector at room temperature and that the resonance frequency could be tuned by the gate bias.

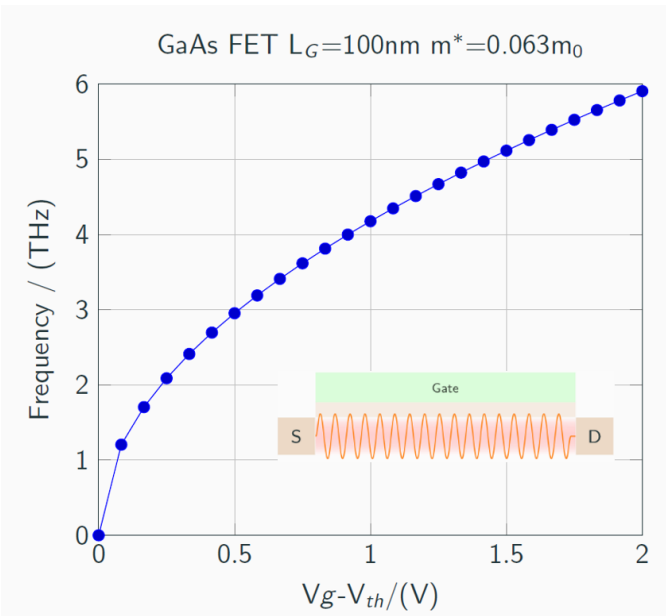


Figure 1.2 Resonance frequency as function of the gate voltage swing for a GaAs FET

The equations describing the 2D plasmons are the relationship between the surface carrier concentration (n_s) and the swing voltage (U_0) (Equation 1.2), the equation of motion (Euler equation, equation 1.5), and the continuity equation (Equation 1.6).

$$\frac{\partial U}{\partial t} + \frac{\partial (Uv)}{\partial x} = 0 \tag{1.5}$$

$$\frac{\partial v}{\partial t} = -\frac{e}{m}\frac{\partial U}{\partial x} - \frac{v}{\tau} \tag{1.6}$$

where $\partial U / \partial x$ is the longitudinal electric field in the channel, *v(x,t)* is the local electron velocity, and the last term (v/τ) describes the viscosity and accounts for electron collisions with phonons and/or impurities (τ is the relaxation time). According to Dyakonov & Shur [18], [19] the solution of those equations under the boundary conditions of common-source and open-drain is given by:

$$\Delta U = \frac{U_a^2}{4U_o} f(\omega) \tag{1.7}$$

$$f(\omega) = 1 + \beta - \frac{1 + \beta \cos\left(2k_0^{'} L\right)}{\sinh^2\left(k_0^{''} L\right) + \cos^2\left(k_0^{'} L\right)} \tag{1.8}$$

where:

$$\beta = \frac{2\omega\tau}{\sqrt{1 + (\omega\tau)^2}} \tag{1.9}$$

$$k_0^{'} = \frac{\omega}{s}\sqrt{\frac{\left(1 + (\omega\tau)^{-2}\right)^{-1/2} + 1}{2}} \tag{1.10}$$

$$k_0^{''} = \frac{\omega}{s}\sqrt{\frac{\left(1 + (\omega\tau)^{-2}\right)^{-1/2} - 1}{2}} \tag{1.11}$$

Equation 1.7 describes the response of the device as a THz detector for any frequency and gate length. The function $f(\omega)$ depends on two dimensionless parameters: $\omega\tau$ *(quality factor)* and $s\tau/L$. Figure 1.3 shows $f(\omega)$ as a function of $\omega\tau$ for different values of $s\tau/L$. When $\omega\tau >> 1$ and for submicron devices, such that $s\tau/L >>1$, $f(\omega)$ exhibits sharp resonances at the fundamental frequency and its odd harmonics (Figure 1.3 (a) and (b)). In this case, the damping of the plasma waves excited by the incoming radiation is small and the device exhibits a resonance detection mode. However, when $\omega\tau << 1$, plasma oscillations in the channel are overdamped. For a long device, the oscillations excited at the source by the incoming radiation do not reach the drain because of the damping. The boundary conditions at the drain are irrelevant in this case, and the response does not depend on L. As it can be seen in Figure 1(c) and (d), $f(\omega)$ changes from $f \sim 1$ for $\omega\tau << 1$ to $f \sim 3$ for $\omega\tau >> 1$; we also see how at very small values of $\omega\tau$ the condition of a long sample is violated, and f tends to zero. In both cases, a long channel acts as a broadband detector of electromagnetic radiation. Underdamped ($\omega\tau>>1$) or overdamped ($\omega\tau >> 1$) plasma waves decay near the source end of the channel, leading to a DC voltage induced between drain and source.

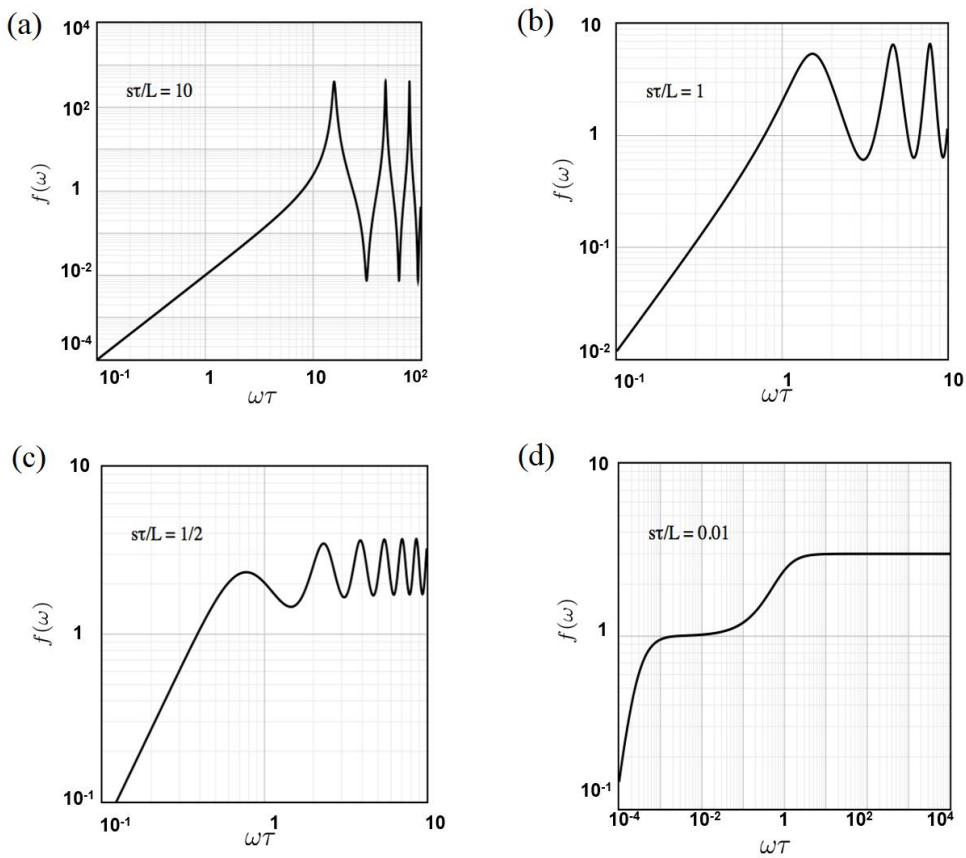


Figure 1.3 Function *f(ω)* as function of different values of *sτ/L*

According to the simple analytical analysis presented in [22], an equivalent circuit of the FET can be given by a RLC ciruit as shown in Figure 1.4; where C is the capacitance gate-channel, R the channel resistance and L the kinetic inductance related to electron inertia that is proportional to the electron effective mass *m*. The operation of the FET as a THz detector will depend on the frequency ω, the gate length *L* and the effective length $L_{eff} = s\tau$ that describes the propagation distance of the waves inside the channel. Hence, it can be divided in two main regimes:

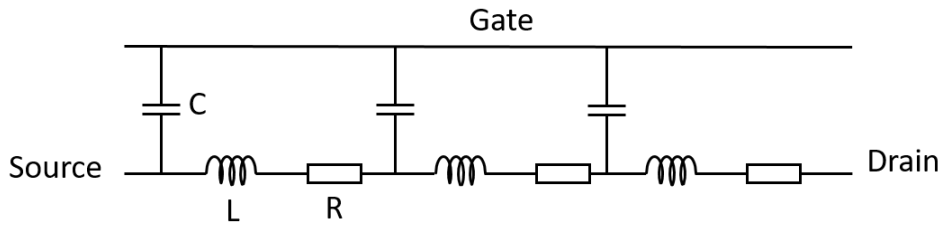


Figure 1.4 Equivalent circuit of FET when used as a detector

1. High frequency regime (ωτ > 1), where τ is again the electron momentum relaxation time, determining the conductivity in the channel σ=ne2C/m. In this case, the kinetic inductances in Figure 1.4 are of primordial importance, and the plasma waves analogous to the waves, in an RLC transmission line, will be excited.

    a. For a short gate, L < L_{eff}, the plasma wave reaches the drain side of the channel, gets reflected, and forms a standing wave with an enhanced amplitude, in these conditions the channel acts as a resonant cavity for the waves. Figure 1.5 shows the dependence of L_{eff} with the frequency for diferent transistors (GaAs FET, Si-CMOS, and Si-MODFET). It is clearly seen that the effective length decreases when increasing the frequency and to reach the conditions for resonant detection, the gate length should be lower than L_{eff}. For example, for our studied transistors (Si-MODFET), the gate length should be less than 80nm at 0.3 THz.

    b. For a long gate, L>>L_{eff}, the plasma waves excited at the source will decay before reaching the drain, so that the AC current will exist only in a small part of the channel adjacent to the source (inset of Figure 1.5).

2. Low frequency regime (ωτ << 1), the plasma is overdamped and at this low frequency regime the impedance of the inductance is low. Hence, the inductance is in short-circuit and the equivalent circuit is mainly an RC circuit. The most relevant parameter is $\omega\tau_{RC}$, where τ_{RC} is the RC time constant of the whole transistor. Since the total channel resistance is Lρ/W, and the total capacitance is CWL (where W is the gate width and ρ=1/σ is the channel resistivity), it can be easily found that $\tau_{RC} = L^2\rho C$.

a. For a short gate, $\omega\tau_{RC}$ < 1, the AC current goes through the gate-to-channel capacitance uniformly across the whole length of the gate. This is the so-called "resistive mixer" regime [23], [24].

b. For a long gate, $\omega\tau_{RC}$ >> 1, the induced AC current will leak to the gate at a small distance l (leakage length) from the source, such that $\tau_{RC} = l^2 \rho C$. If l << L, then neither AC voltage nor AC current will exist in the channel at distances beyond l.

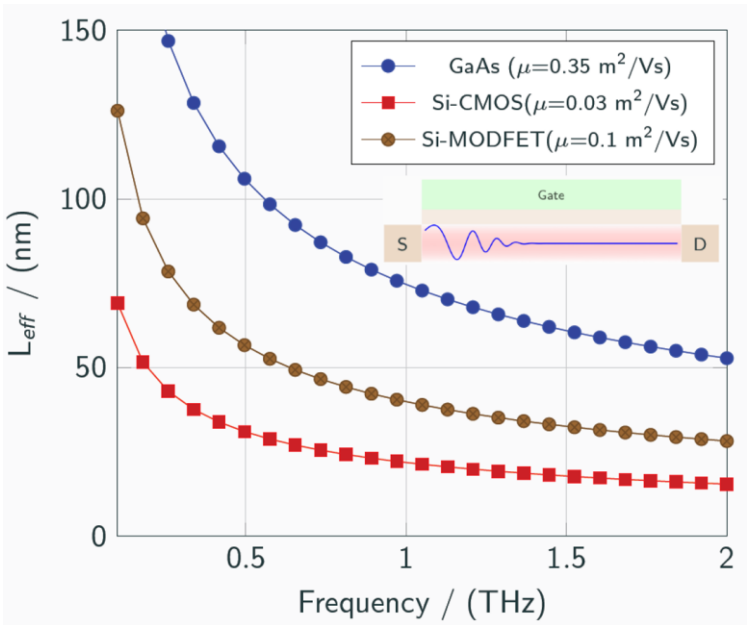


Figure 1.5 Effective length as function of the frequency for GaAs, Si-CMOS and Si-MODFET.

In summary, resonant detection will be observed only if the quality factor is greater than unity and if the gate length of the FET is lower than the effective length given by sτ. In other cases, the detection is non-resonant, and the detector is a broadband one.

Chapter 2

Experimental setup and equipment

This chapter describes the experimental setups used in DC and THz measurements from 4K to room temperature (T_{room}) across this PhD work. Mainly, I have to mainly distinguish between two setups: the low temperature and THz measurements and imaging setup at USAL (University of Salamanca) premises and the THz detection setup at room temperature at CEZAMAT (Centre for Advanced Materials and Technologies, Warsaw, Poland) facilities. Additionally, a brief description of the experimental equipment for detection experiments is described.

Finnally, this chapter will describe the main equipment used for the characterization and fabrication of GFETs in this thesis.

2.1 THz detection system from 4K up to 300K at USAL

This section describes the setup used for DC and THz measurements in the temperature range 4K - 300K. An Optistat AC-V12 cryostat (Figure 2.1) cooled by a closed cycle refrigerator was used. This system is able to cool samples to helium temperatures without the need for liquid cryogens.

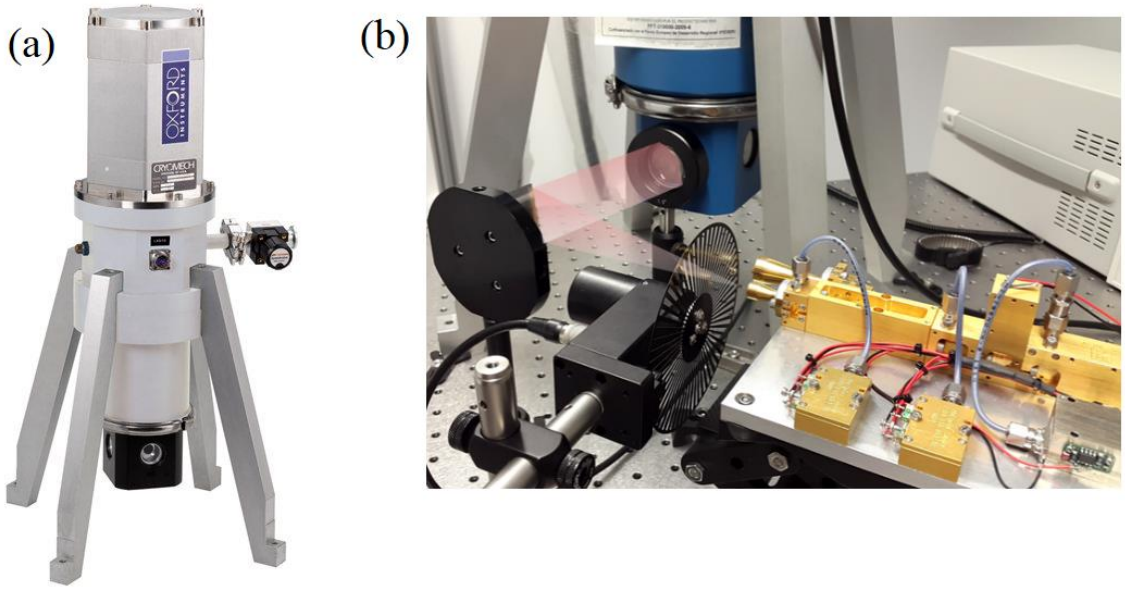


Figure 2.1 Optical cryostat (a) and experimental setup (b) at USAL facilities for measurements in the range from 4K up to 300K.

The cryostat has 4 optical windows, each of them with a diameter of 12.7 mm that are used for the optical access. One of these optical windows was removed and replaced by a Teflon optical window to perform THz measurements and improve our THz setup. Teflon windows ensure that the sample is only excited by the THz radiation, since they

show good transmittances on these frequency ranges making them ideal components for IR and THz applications. Conversely, they exhibit close to zero transmittance in the visible range [25] ensuring that the devices are only excited by the incoming THz radiation. The samples placed on this system are held in vacuum and cooled by a Pulse Tube refrigerator. A temperature controller is used to control heating and thermometry of the sample from 4K up to 325K with a temperature stability of ±0.3K.

In THz experiments, transistors were excited by a RPG (Radiometer Physics GmbH) dual-frequency THz source. It uses a solid-state Dielectric Resonator Oscillator (DRO) at 12.5 GHz and electronic multiplication to generate a THz beam at 0.15 THz with an output power of 3 mW and another one at 0.3 THz with an output power of 6 mW. The output power was measured close to the source using a highly sensitive calibrated pyroelectric detector. For lock-in detection the THz radiation was modulated by a mechanical chopper between 0.1 and 4 kHz and then collimated and focused using an off-axis parabolic mirror and an optical lens.

Figure 2.1 (b) shows a photograph of the experimental bench described above. Since the sample is mechanically fixed into the cryostat it cannot be repositioned, rotated, or tilted, then the THz detection measurements performed on this system were limited. Nevertheless, the source was placed on a XYZ stage manipulator ensuring a proper alignment between the sample and the THz beam.

2.2 THz detection & imaging system at USAL

DC and THz measurements at room temperature performed at the THz Laboratory of the USAL were carried out in an additional optical bench. Figure 2.2 shows a photograph of this bench, (a), along with a scheme of the experimental setup used for the terahertz characterization at room temperature, (b). The DRO-based THz source and the mechanical chopper described in section 2.1. were both used in this system. The output THz radiation was modulated, collimated and focused twice by using an indium tin oxide (ITO) mirror and off-axis parabolic and plane mirrors. The ITO mirror acts as a dichroic mirror since the ITO layer is highly reflective (95%) for the THz beam due to its high conductivity while is highly transparent (80% transmittance) to visible light. This allows the use of a visible red LED (or laser) for the alignment of the THz beam. This experimental setup has two focal points. The second focal point (FP2) is used to place the THz detectors on a XYZθ stage micromanipulator. Optionally, the system has a first focal point (FP1) to place an object that can be moved by using a XY stage. In this configuration, the incoming THz radiation goes through the object placed at FP1 and then the transmitted light is focused again at FP2 and measured with the THz detector using the lock-in amplifier. This configuration allows us to generate a pixel-by-pixel THz photograph of the object placed at FP1.

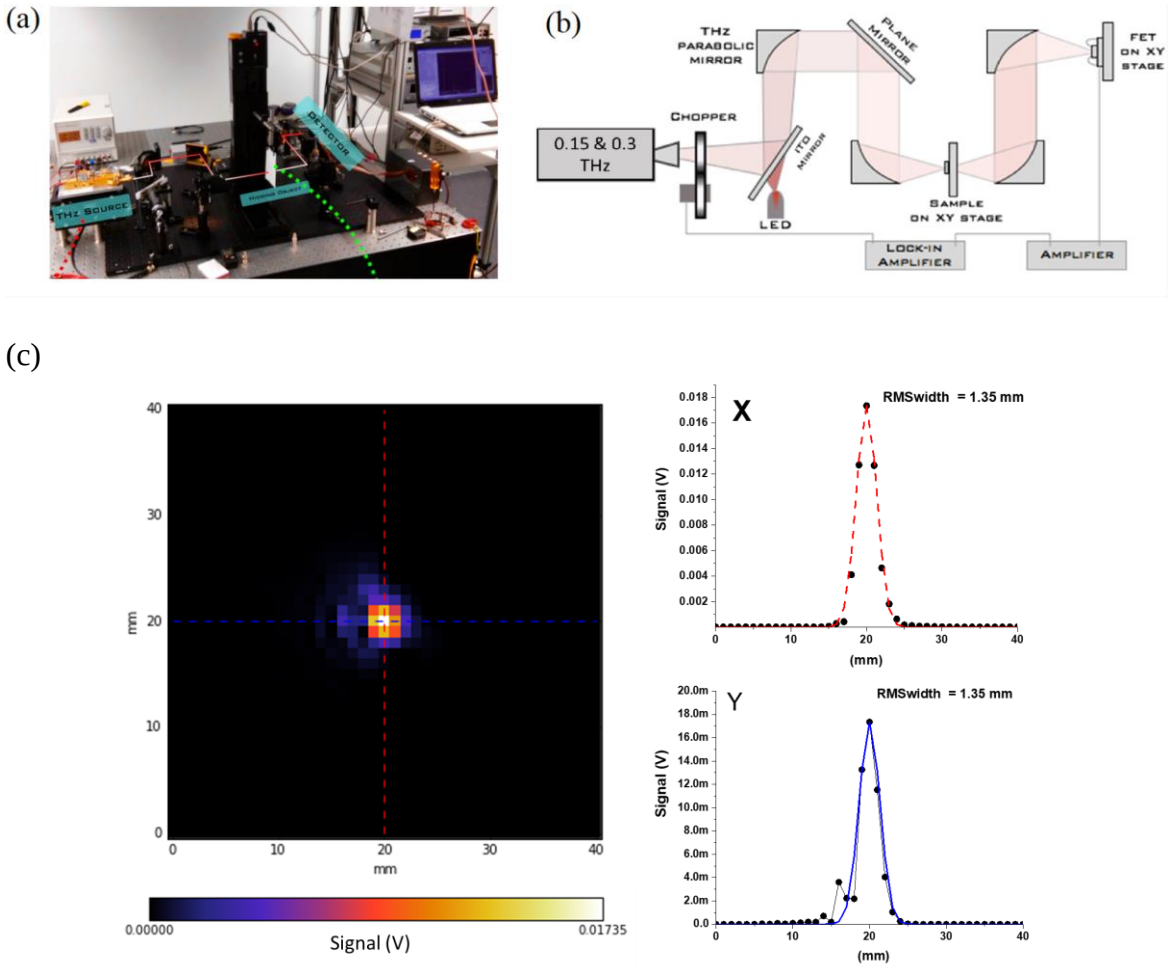


Figure 2.2 Photograph of the experimental bench, (a), schematic, (b) of the THz imaging setup implemented at the USAL Thz Lab, and image of the 0.3 THz beam and its shape profile (c).

The beam power and the spot area of the 0.15 and 0.3 THz EM radiation were measured using a calibrated pyroelectric detector at the FET position (FP2). Power values obtained were 0.5 mW at 0.15 THz and 1 mW at 0.3 THz. The spot area was estimated by taking a pixel-by-pixel image of the beam spot at the FET position. Figure 2.2 (c) shows a homogeneous circular beam spot for the 0.3 THz radiation. A similar shape was obtained for the 0.15 THz beam. The area of the beam spot was estimated to have a size of πr^2, where r is the radius of the beam spot. Values of 1.35 mm for 0.3 THz and 3.3 mm for 0.15 THz were found for r (Figure 2.2 (c) right).

2.3 THz detection & imaging system at CEZAMAT

Broadband THz measurements at room temperature were performed at CEZAMAT facilities. Figure 2.3 shows a picture of the experimental setup used in the detection

experiments carried out at this laboratory. The experimental setup comprised a THz-wave generator from VDI (Virginia Diodes, Inc.) and three Signal Generator Extension Modules offering full waveguide band coverage from 0.140 THz to 0.440 THz:

- WR5.1 140 – 220 GHz (typ. +4 dBm)
- WR3.4 220 – 330 GHz (typ. -2 dBm)
- WR2.2 330 – 440 GHz (typ. -10 dBm)

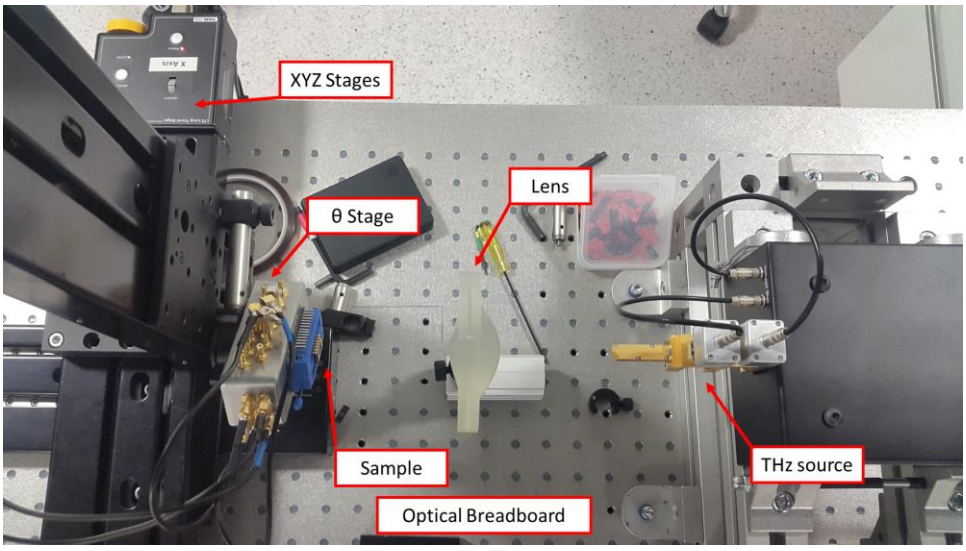


Figure 2.3 Photograph of the experimental bench at CEZAMAT facilities

The vertically polarized output THz beam was focalized on the devices placed at the focal point of the setup by using biconvex polyester/Teflon lenses. Devices were placed on a holder box fixed to XYZθ stages micromanipulators allowing us to perform measurements dependent on the beam polarization.

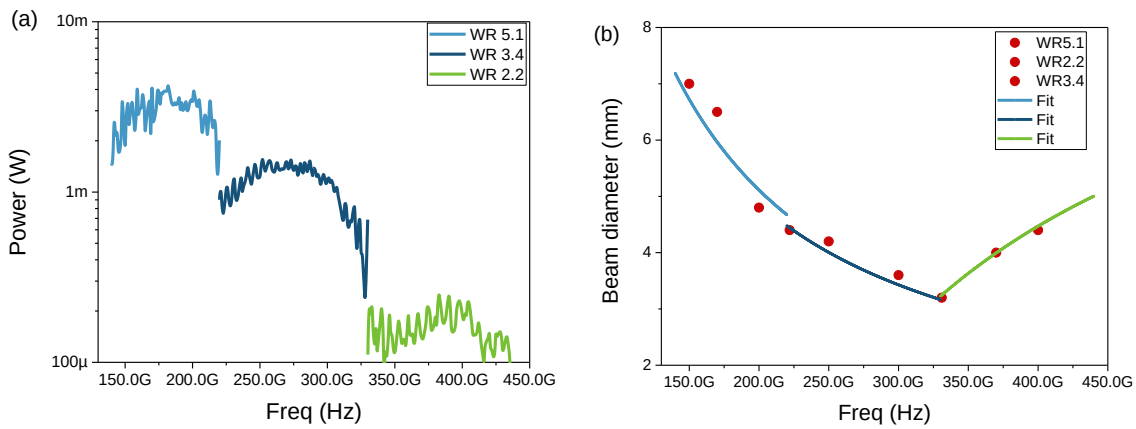


Figure 2.4 Source power (a) and beam diameter (b) as a function of the output frequency in the frequency range from 0.15 up to 0.44 THz.

Figure 2.4 (a) shows the output power while the THz generator was tuned across the full frequency range of the system (140 - 440 GHz). The signal power was measured at the focal point by using a calibrated pyroelectric detector. Since the frequency was tuned, the beam diameter of the THz radiation changes across the frequency range. Its size was again measured at different frequencies (red dots - Figure 2.4 (b)) by taking a XY pixel-by-pixel image of the beam spot around the focal point. Then, different fits were performed for the different frequency ranges measurements to estimate the beam diameter across the full range (Figure 2.4 (b)).

2.4 Fabrication equipment

This section describes the equipment used for the fabrication of the ADGG-GFETs. The equipment is located into the Nanotechnology Clean Room of the USAL.

2.4.1 FE-SEM with Nanolithography Controller

Electron beam lithography processes were performed using a Scanning Electron Microscope (SEM) FE-SEM SIGMA FROM Zeiss with a nanolithography controller (Figure 2.5). The Zeiss Sigma is a SEM with a Schottky Field Emission (FE) source and a GEMINI electron optical column. The instrument has 2 detectors, an In-Lens Secondary Electron detector, lateral Secondary Electron (SE) Detector. Apertures range from 7.5 up to 120 microns and a maximum accelerating voltage of 15kV. The instrument includes 4-axis (x, y, z, θ) fully motorized rotary stages. Samples of size as large as 20 cm are allowed.

Figure 2.5 Lithography system at USAL cleanroom

2.4.2 PlasmaPro 100 Estrelas (Oxford Instruments)

Dry etching processes were carried out on a PlasmaPro 100 Estrelas system (Figure 2.6). The PlasmaPro 100 Cobra from Oxford Instruments allows inductively coupled plasma (ICP) etching as well as Reactive-Ion Etching (RIE). It is designed to perform dry etching of dielectric, compound semiconductor, metals, or organic materials among others.

Figure 2.6 PlasmaPro 100 Cobra system for dry etching

The PlasmaPro 100 Cobra is compatible with samples up to 4-inch diameter. The system is equipped with a cryogenic module allowing to work down to -120 ºC to perform cryoetching. Moreover, it has an interferometer system that allows to full control the etching during the processing.

Several materials can be etched through the different gases lines; Cl_2, BCl_3, Ar, SF_6, $C4F_8$, O_2, CH_4, CHF_3 and H_2.

2.4.3 RTP As-One 100

Annealing processes were performed by using the system Rapid Thermal Processing (RTP) As-One 100 (Figure 2.7 (a)). The system is fully recipe controlled and allows working on a temperature range from room temperature up to 1500 ºC with an accuracy of ± 2 ºC due to an infrared halogen lamp. System heating ramp rates up to 200°C/s and cooling rates up to -100°C/s are allowed. Nevertheless, the maximum process duration is shorter at high temperature due to the cooling capacity of the machine, i.e. at 950 ºC the maximum duration process is limited to 3 hours and at 1500 ºC the maximum duration is limited to 30 seconds.

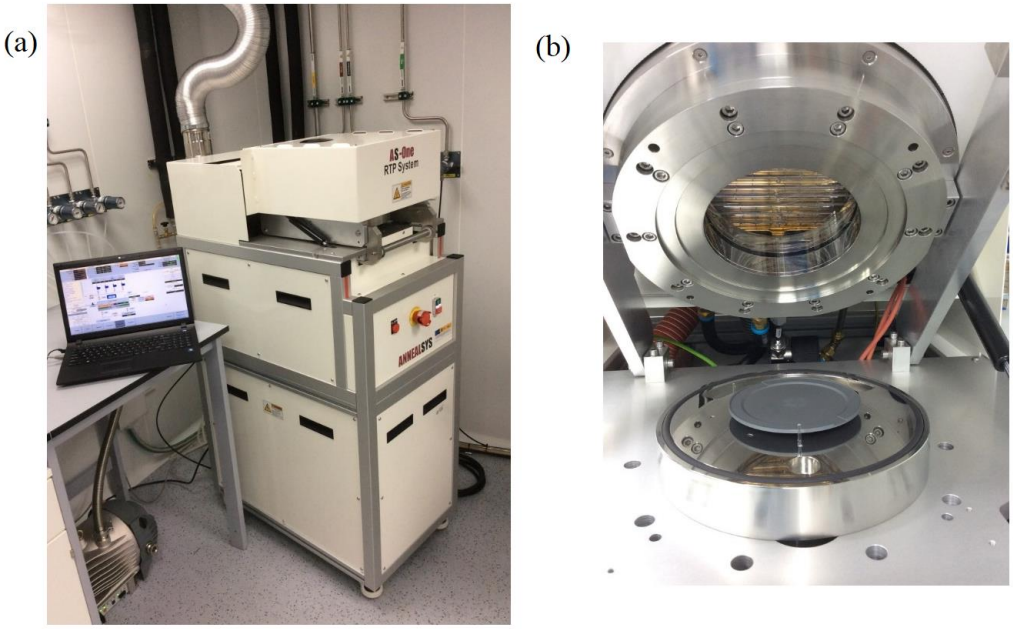


Figure 2.7 Thermal annealing system at the USAL cleanroom

The system is equipped with a chamber designed to process substrates up to 100 mm (4-inch wafers) diameter (Figure 2.7 (b)) and can operate under atmospheric pressure or under vacuum (10^{-6} Torr). Small substrates can be introduced using susceptors. The system is equipped with 4 lines of gases (N_2, O_2, Ar, He) allowing to modify the environment and flushing the sample during the annealing process.

2.4.4 e-beam Evaporator

Metallization of graphene-based devices was performed by using an e-beam evaporator (Figure 2.8 (a)). This e-beam system is designed with two independent chambers and can be isolated or connected using a manual guillotine. The large main chamber is habitually under high-vacuum (10^{-9} mbar). Conversely, a small secondary chamber (load-lock) is connected (isolated by the guillotine) to the main chamber working in a pressure range from atmospheric pressure down to 10^{-6} mbar. The small volume of the secondary chamber allows to reach 10^{-6} mbar pressure in relatively short times (less than 30 minutes) and then load (or unload) the samples into (or from) the main chamber while keeping the main chamber under high-vacuum. The e-beam evaporator has a long distance between the target and the sample (> 0.5 m) and works at very low pressures to ensure a high control on the evaporation rate (less than 1 Å/s) to create high homogeneity thin films on the sample. The evaporation rate, as well as the evaporated metal thickness, is controlled by a quartz crystal. The system is equipped with an e-beam gun from Telemark with a tungsten filament.

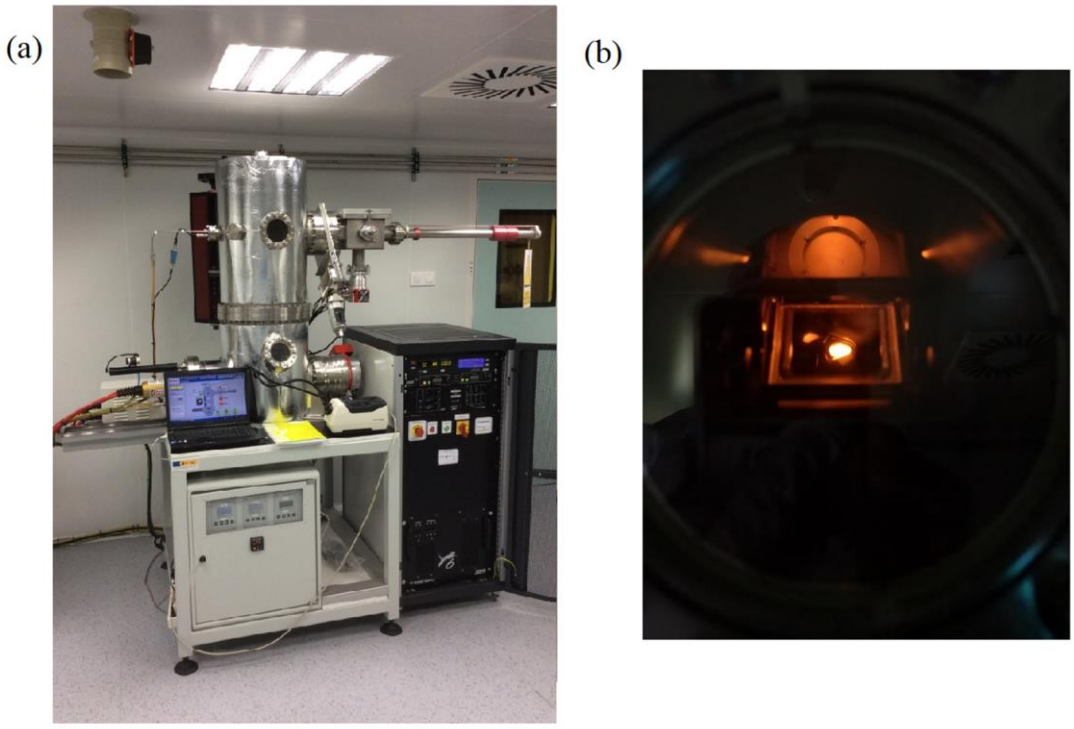


Figure 2.8 Photograph of the e-beam evaporator (a) and gold heated up by the electrons beam (b)

By applying a small emission current to the filament, electrons are accelerated by high voltage (8 kV) and leaded by the magnetic field to the center of the pocket with the desired metal (target). Other low intensity magnetic field known as "XY Sweeping" can be used to move the e-beam diffusing the energy to heat the target material more evenly. Finally, the metal is heated up as the emission current is increased (Figure 2.8 (b)), converting it to a gaseous state and then precipitate it to form a thin film coating the sample.

Several metals can be evaporated in the system using the e-beam evaporator (Au, Ti, Al, Cr, Co, Ni, Pt) as well as some dielectrics (SiO_2, Al_2O_3, HfO_2).

2.5 Characterization equipment

This section will describe in more detail the equipment used in this PhD for the device characterization. This equipment includes the one used for material characterization and for DC and THz measurements.

2.5.1 Profilometer

Profile measurements were performed by using a DektakXT® stylus surface profiler (Figure 2.9). The DektakXT is an advanced thin and thick film step height measurement tool. In addition to profiling surface topography and waviness, the DektakXT system measures roughness in the nanometer range. It has automatic X-Y-theta stages and provides a step-height nanometer resolution.

In addition to taking two-dimensional surface profile measurements, the DektakXT system can produce three-dimensional measurements creating 3D Maps.

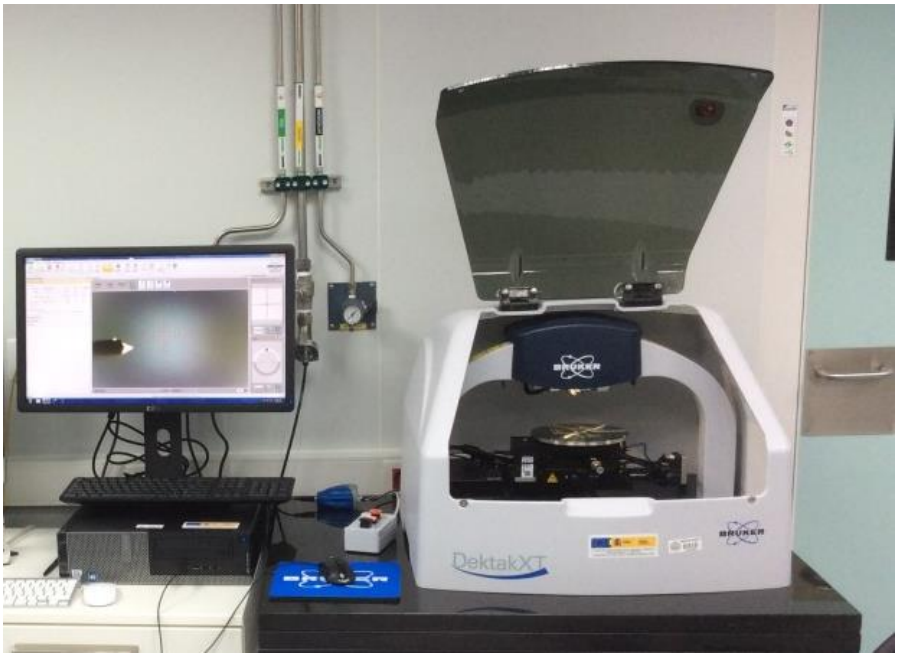


Figure 2.9 Photograph of the DektakXT profilometer system

The DektakXT system takes measurements electromechanically by moving a diamond-tipped stylus over the sample surface according to a desired scan length, speed and stylus force. The stylus is linked to a Linear Variable Differential Transformer (LDVT), which produces and processes electrical signals that correspond to surface variations of the sample. After being converted to digital format, these surface variations are stored for display and analysis. The Vision64 application calculates and displays the results of user-selectable analytical functions for measuring surface texture and other parameters to characterize the profile data.

2.5.2 Micro Raman Spectrometer (LabRAM HR Evolution)

Raman measurements were performed by using the Micro Raman Spectrometer – LabRAM HR Evolution (Figure 2.10). The LabRAM HR system is suited to both micro

and macro measurements, offering confocal imaging capabilities in 2D and 3D. It is equipped with three different lasers:

- Ventus Solo laser at 532 nm with an output power of 100 mW
- He-Ne laser at 633 nm with an output power of 17 mW
- Diode laser at 770-795 nm with an output power > 200 mW

The LabRAM HR system is suited to both micro and macro measurements since it is equipped with an objective (100x) designed with short free working distance and two objectives (10x and 50x) with long working distance. Measurements performed in this PhD were carried out with the 100x objective distance due to the micro nature of the 2D materials. The 100x objective produces laser spots as small as ~ 1 μm^2 at the focal distance. Incident light can be attenuated till values of 0.01% of the output power. Raman measurements can be performed on the frequency shift range from a relatively low wavenumber cut-off of 50 cm^{-1} and with an accurate step below of 2 cm^{-1}.

Figure 2.10 Photograph of the Raman spectrometer at USAL facilities

Samples are placed on a XY motorized stage with 0.05 μm X-Y step that enables to perform fast confocal Raman imaging measurements. The collection of the scattered light is made with confocal geometry, namely backscattered light is collected by the same objective that focuses the exciting laser beam. Two different diffraction gratings can be used with 1800 grooves/mm or 600 grooves/mm. Raman spectrums are collected by using a 256x1.024 pixels Synapse CCD detector (with a spectral range of 200-1.050 nm) that is cooled by Peltier effect.

2.5.3 Lock-in Amplifier & Keitley 2410

The experimental data about electrical characterization presented in this Thesis were acquired using either lock-in amplifiers or Keithley sourcemeters, which are capable of measuring small signals adding extremely low noise levels. DC measurements were performed by using double channel Keithley 2412 sourcemeter units (SMU) (Figure 2.11 (a)). This SMU provides precision voltage and current sourcing as well as measurement capabilities.

Lock-in amplifiers where employed for AC/DC measurements in THz detection experiments. The lock-in amplifiers employed are the model Stanford Research SR830 as the one showed in Figure 2.11 (b). An alternate AC signal is collected by the input channels (current or voltage can be used) and filtered by the amplifier. The filtering works in such a way that the only component which is selected by the instrument has the same frequency than a reference signal to which is phase-locked (i.e. has a phase relation which is fixed in time). This reference signal can be external (i.e. the signal frequency of the mechanical chopper) or generated by the lock-in amplifier itself. This method is known as phase-sensitive detection (PSD). All the other components of the input signal are filtered out, resulting in efficient noise rejection and high accuracy.

(a) (b)

Figure 2.11 Photograph of the Keithley 2412 (a) and Lock-in SR830 (b).

The PSD relies on simple trigonometry, as explained in the following. Considering that an input signal (V_{sig}) can be writen as $V_{sig} \sim \sin(\omega_r t + \theta_{sig})$ and the sinusoidal reference signal (V_L) as $V_L \sim \sin(\omega_L t + \theta_{ref})$. The two signals are multiplied by the lock-in; the resulting signal is as follows:

$$\frac{1}{2}V_{sig}V_L\cos((\omega_r-\omega_L)t+\theta_{sig}-\theta_{ref})-\frac{1}{2}V_{sig}V_L\cos((\omega_r+\omega_L)t+\theta_{sig}+\theta_{ref}) \quad \textbf{(2.1)}$$

The output signal described by Equation 2.1 consists of two sinusoidal signals, one at the frequency that is the difference of the two input frequencies ($\omega_r - \omega_L$), and one at the sum of these frequencies ($\omega_r + \omega_L$). When the input signal has the same frequency than the reference signal (i.e. $\omega_r = \omega_L$), the difference signal becomes a DC value. When the PSD output is passed through a low pass filter, the component ($\omega_r + \omega_L$) is filtered out and the resulting signal is as follows:

$$\frac{1}{2}V_{sig}V_L\cos(\theta_{sig}-\theta_{ref}) \tag{2.2}$$

Equation 2.2 shows that the intensity of the resulting DC signal is proportional to the input signal's one (V_{sig}). All the components at frequencies other than the one of the reference are filtered out. By adjusting θ_{ref} on the lock-in amplifier we can make $\theta_{sig} = \theta_{ref}$ and the difference will be equal to zero; in this case the resulting signal is directly proportional to V_{sig} and can be measured. Conversely, if the difference between θ_{sig} and θ_{ref} is equal to $\pi/2$, the output signal will be equal to zero.

Chapter 3

Silicon FETs

3.1 Introducción

Semiconductor plasmonic FETs operating as detectors in the THz range has been demonstrated [26]. FETs fabricated on III-V compounds [27],[28] or silicon [29] are the two principal researching lines in solid-state plasmonic THz detectors. Nevertheless, one of the major advantages of employing Silicon FETs lies in the capability to produce low cost, scalable and reliable commercial THz technology. Moreover, to facilitate this task, the development of THz devices can be complemented with accurate simulations. This can be performed by using different tools such us the Technology Computer-Aided Design (TCAD) Synopsys simulator [30] to obtain the performance of the device for both DC and AC simulations. This chapter addresses the study of two different silicon-based devices as THz detectors. The first one lies with the theoretical and experimental studies of strained-Si MODFETs. An analysis employing Synopsys TCAD was performed. The second one is the use of silicon FINFET devices.

3.2 Si/SiGe technology

Throughout this section we will present some basic concepts about the Silicon (Si), Germanium (Ge) and Si/SiGe systems necessary to understand the behavior of the transistors showed in this chapter. As these transistors rely upon the strain of a pure-Si layer sandwiched between relaxed layers or SiGe a right understanding of the properties of the. Si/SiGe material system is necessary

Accordingly, the most basic properties (mobility, GAP, band structures, …) of the two simple semiconductors (Si and Ge) will be presented. Also, the properties of Ge/SiGe and Si/SiGe heterojuncions will be revised. A particular emphasis will be placed on the influence of strain on the heterojunctions (valence and conduction bands offset, mobility, …).

3.2.1 Si, Ge and SiGe systems

The crystal structure of silicon and germanium is classified under the diamond structure, and thus it has two atoms in a primitive cell: The crystal lattice can be represented as two interpenetrating face centered cubic lattices (FCC) with a cube side of 0.543 nm in the case of Si and 0.566 nm in the case of Ge (Figure 3.1). The structure is visualized as a tetrahedron with four vertices of the first FCC lattice at (0,0,0), (a/2,0,0), (0,a/2,0) and (0,0,a/2) and an additional atom added to the center of this tetrahedron. The additional lattice is displaced diagonally by 1/4 with respect to the first FCC lattice.

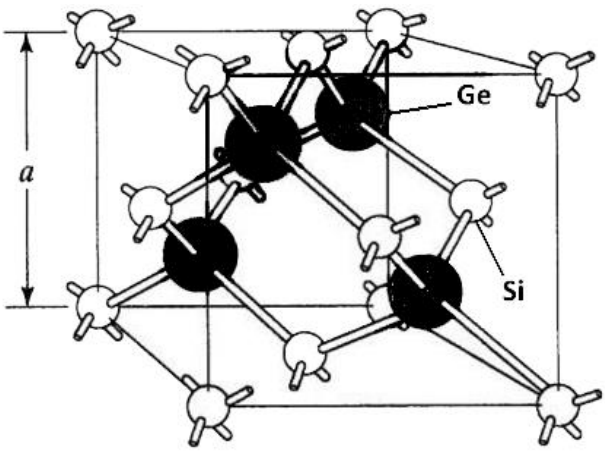


Figure 3.1 The unit cell and diamond lattice structure for Si, SiGe, and Ge [31]

In silicon, the conduction band minima (Figure 3.2 (a)) lie on the six equivalent Δ-lines along the <100>-directions and occur at about 0.85% of the way to the Brillouin zone boundary (Figure 3.3 (a)), i.e. near the X points of the first Brillouin zone, the minima are called X- valleys. In bulk Ge the eight equivalent minima lie in the L points, i.e. in the limit of the Brilloin cell (Figure 3.3 (b)).

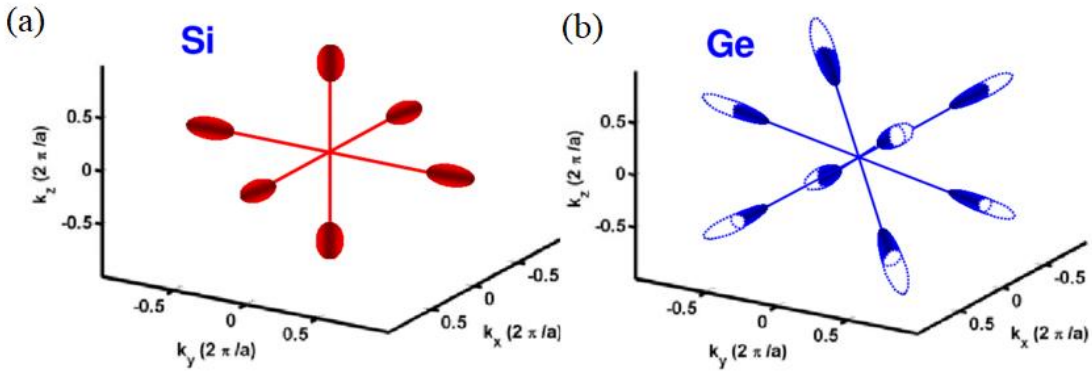


Figure 3.2 Si (a) and Ge (b) equi-energy valleys. [32]

The material system $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ is used to fabricate high-speed transistors based in the heterojunction between both materials alloys. The flexibility of the material system allows the design of FETs and HBTs (Heterojunction Bipolar Transistors) by controlling the values of the molar fraction at each side of the heterojunction, the vertical doping profile and the epitaxial growth as one of the layers must be under strain. We will limit ourselves to describe the specific system used in the transistors that this work deals with.

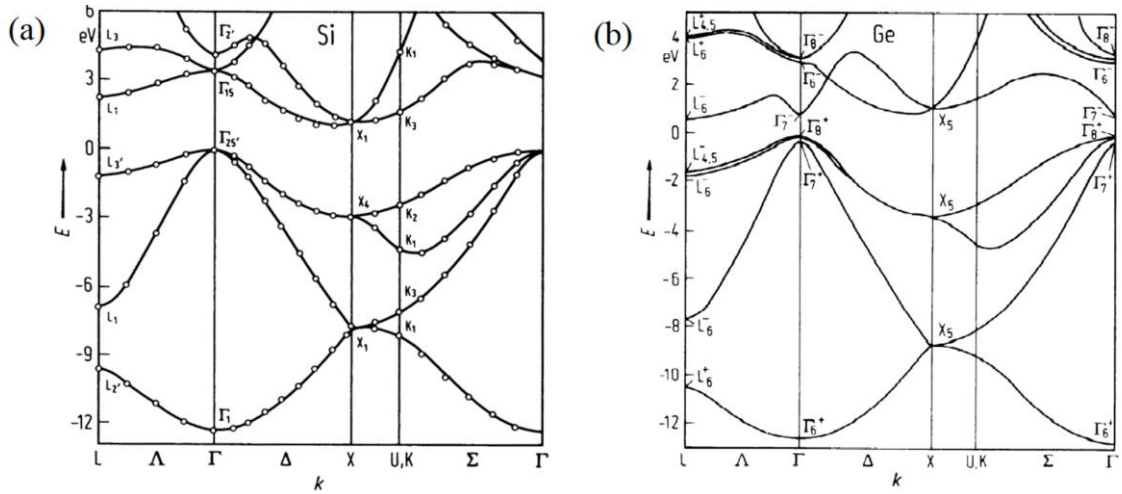


Figure 3.3 Band structure of Si (a) and Ge (b) [33]

The study of bulk (unstrained) $Si_{1-x}Ge_x$ shows that as the molar fraction of Ge is increased, the values of the bandgap and the energy band structure are modified, this has a large impact, for instance, on carrier mobility. As above stated, since we are dealing with n-channel devices we will restrict the scope of this Thesis to the analysis and discussions of electrons in the conduction band. $Si_{1-x}Ge_x$ alloy with Ge molar fractions below 0.85 has a band conduction essentially equal to the one of bulk Si, accordingly the electron masses are essentially the same than in Si and the only noticeable change for electrons is the value of the bandgap. The dependence of this latter with the molar faction approximately follows the Vegard's rule:

$$E_{GAP} = 1.12 - 0.41x\ eV \quad (x < 0.85) \tag{3.1}$$

$$E_{GAP} = 1.86 - 1.2x\ eV \quad (x > 0.85) \tag{3.2}$$

For Ge molar fractions larger than 0.85 the SiGe the conduction band is alike the one of germanium. Both equations are experimentally verified (see Figure 3.4):

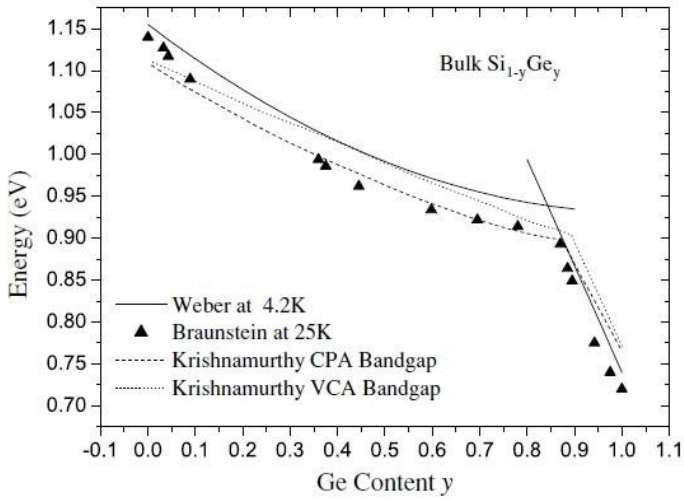


Figure 3.4 Energy GAP on Bulk $Si_{1-x}Ge_x$ at low temperature [34]

Figure 3.4 shows the dependence of the energy bandgap with the molar fraction of Ge in a $Si_{1-x}Ge_x$ alloy. The weak dependence of the bandgap on temperature for a given value of the molar fraction follows the empirical rule:

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta} \tag{3.3}$$

the parameters are given in Table 3.1:

	Germanium	Silicon
$E_G(0)$ (eV)	0.7347	1.166
α (eV/K)	$4.77 \cdot 10^{-4}$	$4.73 \cdot 10^{-4}$
β (K)	235	636

Table 3.1 Constant parameters for the Energy GAP of Ge and Si

Since SiGe technology bears a great interest for cryogenic and aerospace applications the bandgap dependence on temperature is of interest [35]. Nevertheless, in this Thesis we focus on studies at room temperature.

3.2.2 Strain on SiGe composite

Epitaxial growth of $Si_{1-x}Ge_x$ layers can be performed over Si or Ge substrates allowing to obtain almost any composition in the range of $0<x<1$. Since the grown layer has a different lattice constant than the substrate, the upper layer will undergo a

mechanical strain. A higher lattice constant of the grown layer than the one of the substrate will lead to a compressive strain of the crystal unit cell in the normal plane (Figure 3.5 (a)). Conversely, a lower lattice constant of the grown layer will produce a tensile strain in that plane (Figure 3.5 (b)).

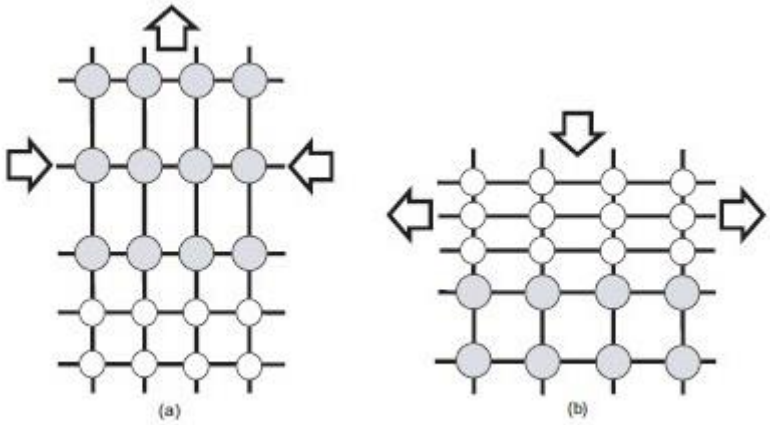


Figure 3.5 Compressive (a) and tensile (b) strain

When the growth is not performed appropriately, the strain can be total or partially relaxed creating dislocations, changes in the symmetry plane, etc. that are highly harmful for the charge transport, downgrading the performance of the devices fabricated with such heterostructures. A high-quality strained layer is achieved by an elastic deformation of the unit cell during the growth of the epitaxial layer (this is indicated in Figure 3.5 by the vertical arrows).

The strain parameter $\left(\bar{\varepsilon}\right)$ is defined as:

$$\bar{\varepsilon} = \frac{a_{substrate} - a_{layer}}{a_{substrate}} \qquad \textbf{(3.4)}$$

Where, $a_{substrate}$ is the lattice constant of the substrate, and a_{layer} is the lattice constant of the layer grown on the substrate. The strain parameter provides information about the magnitude of the mismatch between the epitaxial layer and the substrate. Also, its sign indicates if the strain is compressive (negative strain) or tensile (positive strain). For $Si_{1-x}Ge_x$ alloys, the lattice constant of the compound will increase with the value of the molar fraction as given by the Vegard's law [36]. There are two components of the strain:

- *Hydrostatic strain*, also called volumetric strain or dilatation, is a strain that is equal in all normal directions, with no shear components. It is a change in the volume of a body (in our case this is represente by the unit cell), but not in its shape (Figure 3.6 (a)).

- *Uniaxial* (or biaxial) strain occurs when only one (or two) component of the principal strains is nonzero, changing both the volume of a body and its shape (Figure 3.6 (b)).

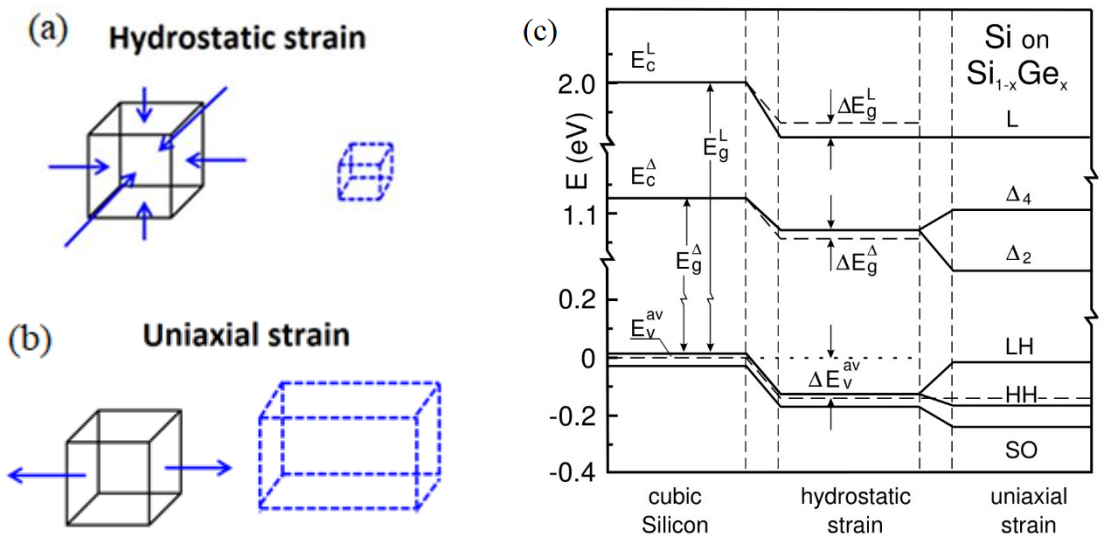


Figure 3.6 Hydrostatic (a) and Uniaxial strain (b). Contribution of the hydrostatic and uniaxial strain on Si growth on $Si_{1-x}Ge_x$ (c)

The hydrostatic strain component leads to an overall downward shift of the average valence band level E_v^{av} by ΔE_v^{av}, but also modifies the Δ and L bandgaps by, respectively, the amounts of ΔE_g^{Δ} and ΔE_g^{L}, respectively (Figure 3.6 (c)). The energy would be determined by the strain parameter. For Si grown on bulk $Si_{1-x}Ge_x$, since the lattice constant of Si is lower than the one of the SiGe substrate the epitaxial Si layer is under biaxial tensile strain. In this configuration, the degenerated Δ_6 valleys of the Si layer are split into four equivalent valleys (Δ_4) which are shifted up in energy, and two equivalent valleys (Δ_2) which are shifted down in energy (Figure 3.7 (a)). In unstrained Si and Ge, the heavy-hole (HH) and light-hole (LH) bands are degenerated at the Γ point. Biaxial strain splits the degeneracy by shifting the HH band below the LH band though the designation of "light" and "heavy" loses its meaning, since the hole effective masses become highly anisotropic with strain [37].

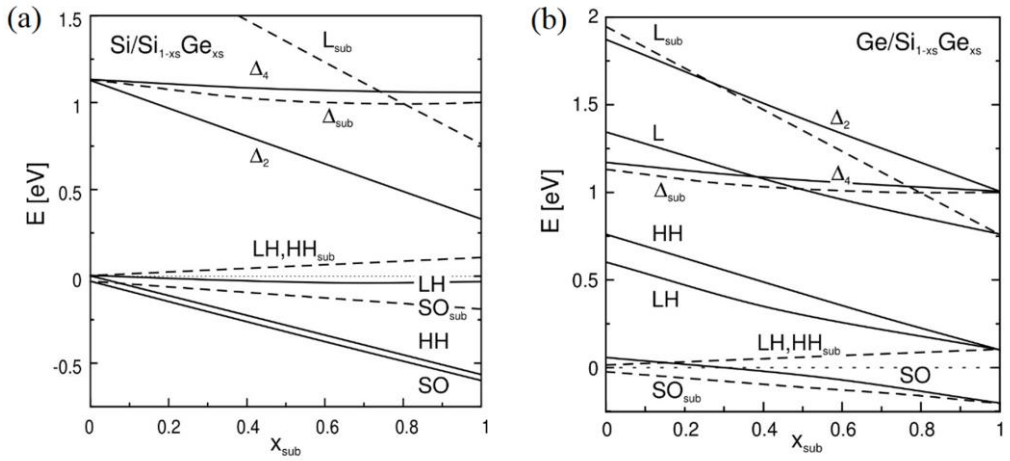


Figure 3.7 Conduction and Valence energy shifts for Si/ $Si_{1-x}Ge_x$ (a) and Ge/ $Si_{1-x}Ge_x$ (b) [38].

An opposite behavior is found in the case of a biaxial compressive strain (i.e. Ge on $Si_{1-x}Ge_x$) where the Δ_4 valleys are shifted down in energy, while the Δ_2 valleys are shifted up. In the case of the valence band, the HH band moves above the LH band (Figure 3.7 (b)).

Since in strained materials both valence and conduction bands are shifted in energy the bandgap is modified. Figure 3.8 shows the variation of the bandgap of strained-Si and strained-Ge_xSi_{1--x} layers versus the Ge molar fraction.

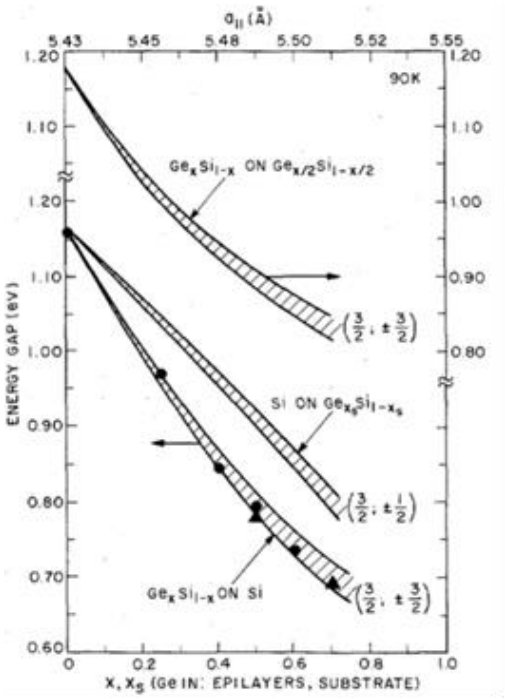


Figure 3.8 Energy Gap shift of Si/Ge composites [39]

A thin layer of $Si_{1-x}Ge_x$ grown on a substrate with lower lattice constant (i.e. Si), produces a biaxial compressive strain on the upper layer. Figure 3.9 (a) shows the offsets produced on the conduction and valence bands when a strained thin $Si_{0.7}Ge_{0.3}$ layer is grown on a relaxed Si substrate. A small offset of 30 mV is produced on the conduction band while a significant energy discontinuity (an offset of 230mV) results in the valence band. This type of heterostructures is useful to build p-FETs as holes can be confined.

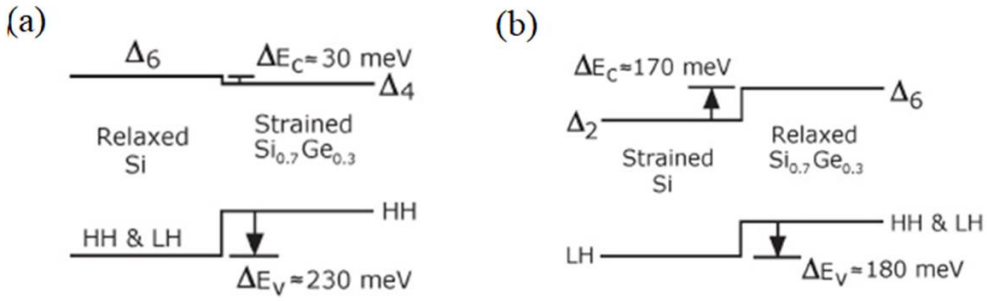


Figure 3.9 Compressive (a) and tensile (b) strain

In a similar way, a thin layer of Si can be grown under tensile biaxial strain on a relaxed SiGe (usually called virtual substrate as SiGe wafers do not exist). Figure 3.9 (b) shows the offset generated on the conduction and valence bands of a heterojunction formed bu growing a strained-Si layer on a relaxed $Si_{0.7}Ge_{0.3}$ virtual substrate. Unlike the compressive strain case, under tensile strain large offsets are obtained for both conduction (170 mV) and valence (180 mV) bands allowing the confinement electrons and holes. Thus, these types of junctions are useful to build p- and n- FETs. A pure strained-Si channel will allow excellent electron mobility as compared to SiGe channels since no alloy carrier scattering will be present. As above pointed out no real substrates of $Si_{1-x}Ge_x$ exist. Therefore, strained-Si/$Si_{1-x}Ge_x$ junctions are fabricated as follows: a conventional silicon wafer is used as the starting substrate and then a thick $Si_{1-x}Ge_x$ layer is grown gradually increasing the Ge molar fraction from zero till the desired final molar fraction. Then a relatively thick layer of relaxed $Si_{1-x}Ge_x$ with a uniform Ge molar fraction is grown on the graded SiGe layer to act, as a relaxed virtual substrate (usually knows as the set back layer). Finally, the strained Si layer is grown on this virtual substrate.

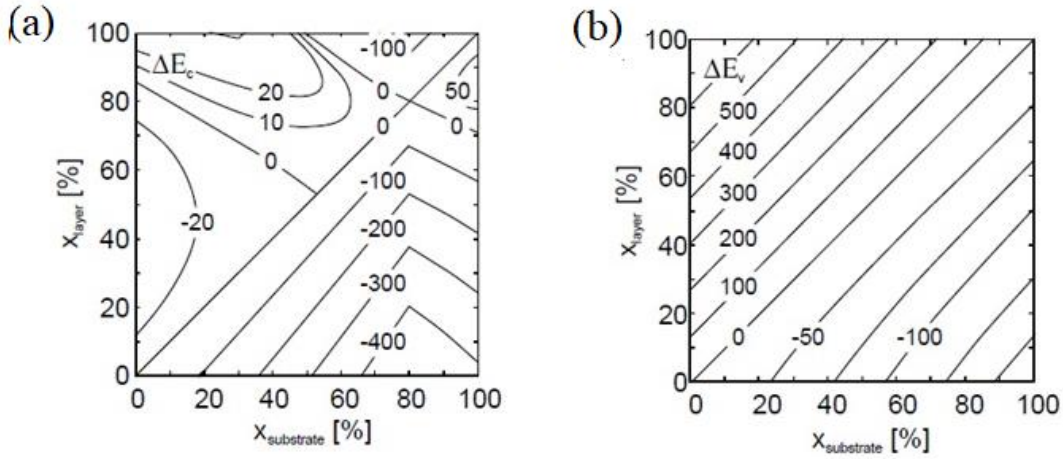


Figure 2.10 Conduction and Valence offsets as function of the molar fraction on the substrate [38]

Figure 3.10 shows the distribution of the theoretical offsets of both conduction (a) and valence (b) bands for strained $Si_{1-xlayer}Ge_{1-xlayer}$ grown on $Si_{1-xsubstrate}Ge_{xsubstrate}$. There are considerable disagreements between theoretical and measured valence band-offset values in literature [38], [40], [41].

3.2.3 Strain and mobility

There are important parameters such as doping density profiles, type of carriers, interface quality, oxide trap density, semiconductor bulk defect density among other that assess the material quality. Nevertheless, the most important transport parameter in a semiconductor is carrier mobility [42]. Carrier mobility can be obtained using a simple model which gives the approximate relation between scattering time (average time between scattering events) and mobility by the next equation:

$$\mu = q\frac{\tau}{m*} \tag{3.5}$$

where q is the absolute value of the elementary charge, m* is the carrier effective mass, and τ is the average scattering time. Since mobility has been always a key parameter to properly desing high-performance semiconductor devices, there is a huge interest in the development of theoretical models to describe the dependence of carrier mobility on electric field, temperature, doping concentration, etc. An accurate estimation of the theoretical maximum values of mobility (of holes and electrons) can be obtained in bulk materials like Si, Ge and then estimate the expected mobility values in strained-Si/SiGe heterostructures [43].

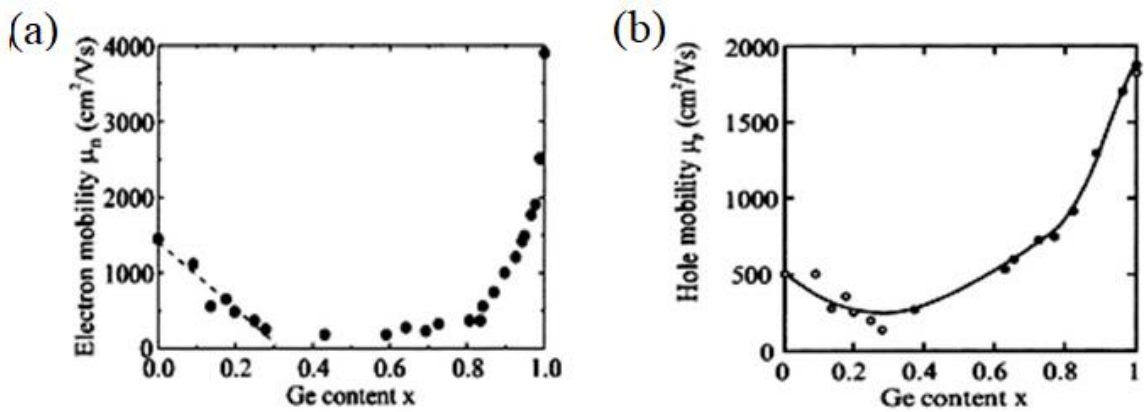


Figure 3.11 $Si_{1-x}Ge_x$ Electron (a) and hole (b) Hall mobility vs composition at 300 K [43]

Figure 3.11 shows the electron (a) and hole (b) Hall mobility as a function of the Ge molar fraction in relaxed $Si_{1-x}Ge_x$. Electron mobility decreases abruptly from the pure materials (Si or Ge) and drops by two orders of magnitude for Ge molar fractions in the range of $0.3<x<0.8$. A similar behavior is found in hole mobility

As described above, biaxial strain results in changes on the conduction and valence bands of Si that directly affect carrier mass, effective density of states and, eventually, intra- and inter- valley scattering.

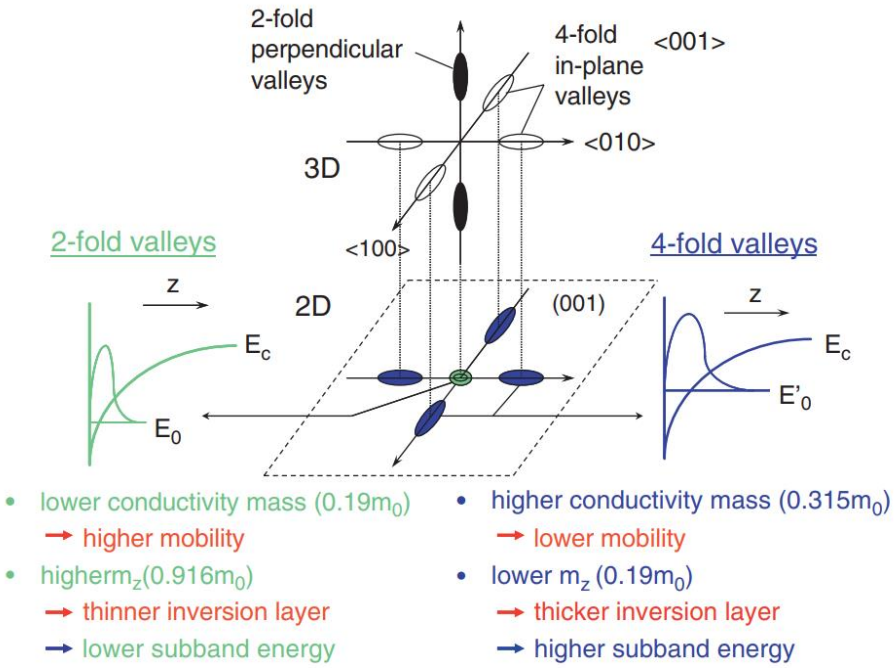


Figure 3.12 Schematic diagram of characteristics of the two- and four-fold valleys in two-dimensional electrons on a (100) surface [44], [45].

In a thin strained-Si layer, electrons essentially exhibit the same anisotropy in their effective mass than in bulk Si [46]. It is composed of two light transversal effective

masses, m_t = 0.19 m_0, where m_0 is the electron mass in free space, and a heavy longitudinal effective mass, m_l(= 0.916 m_0). As a result, the twofold degenerate valleys have the effective masses of m_t in parallel and m_l in perpendicular to the heterojunction interface, while the fourfold degenerate valleys have m_t and m_l effective masses in parallel and m_t in perpendicular to the heterojunction interface. These differences in the effective mass leads to a variety of differences in physical properties between the twofold and the fourfold valleys. For instance, the conductivity mass parallel to the heterojunction interface is lower in the twofold valleys than in the fourfold valleys and, thus, the mobility of electrons in the twofold valleys is higher than the one in the fourfold valleys.

An epitaxial thin layer of Si on unstrained $Si_{1-x}Ge_x$, as Si has a shorter lattice constant than the one of SiGe, Si is under biaxial tensile strain. Accordingly, the strain splits the six equivalent valleys at the minima of the conduction band into twofold perpendicular and fourfold in plane valleys leading to an increase of the mobility through two mechanisms. The first one is the increase of the occupancy of the twofold valleys leading to a lower conductivity mass than in bulk Si and, then, to an improvement of the electron mobility (Figure 3.13). The second one is the suppression of inter-valley scattering between the twofold and the fourfold valleys [45] when carriers are drifted by low and moderate longitudinal electric fields in a FET.. Conversely, biaxial compressive strain leads to a decrease in electron mobility. because the lower energy of the four-fold valleys and thus a higher occupancy of the electrons in valleys having high conductivity mass.

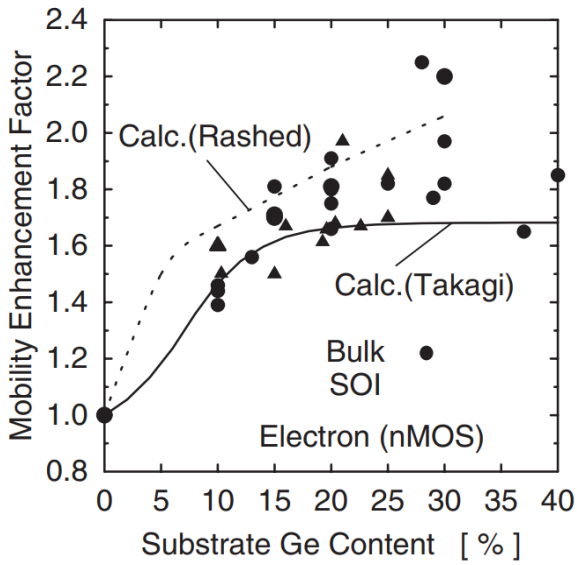


Figure 3.13 Mobility enhancement factor vs Ge molar fraction on strained-Si [45].

The relationship between electron mobility in n-channel Si/SiGe devices has been systematically investigated by using strained-Si FETs fabricated on relaxed SiGe substrates. Figure 3.13 shows experimental results for the mobility enhancement factor [45], defined as the ratio of the mobility in strained-Si MOSFETs and that in conventional (unstrained) Si FETs, as a function of the Ge content of the substrate. Theoretical results forecasting a mobility enhancement factor are also shown [47].

Agreement between the experimental and theoretical results is fairly good. An enhancement factor of roughly two is obtained.

3.3 Strained-Si MODFETs

3.3.1 Introduction

A modulation-doped FET (MODFET) or High-electron mobility FET (HEMT) is a field-effect transistor consisting of a junction between two different materials with different band gaps, creating a heterojunction with a non-doped layer called the channel. Electrons (or holes) are supplied by a high doped layer, usually degenerated and relatively thin called supply-layer, close to a heterojunction, and transferred to the channel. This electron (or hole) transfer is allowed since the discontinuities created as consequence of the different energy on the conduction (ΔEc) and valence bands (ΔEv).

MODFETs present several advantages; they have high gain, so they are useful as amplifiers; a high switching speeds can be achieved since the main charge carriers in MODFETs are majority carriers, and minority carriers are not significantly involved as consequence of the different energy bands; and extremely low noise values because the current variation in these devices is low compared to other FETs.

There are several material combinations to design a MODFET. One of them is based on the SiGe technology. Three different Si/SiGe based MODFETs can be designed. N-channel- or n-MODFETs are based on strained-Si channels [48], [49] and the channel on p-MODFETs are based on SiGe or Ge, with, usually, a molar fraction of 30% [50], [51]. This chapter focuses on n-channl strained-Si MODFETs with two different highly doped supply layers near to the nominally undoped silicon channel.

3.3.2 Device description

N-channel devices under study in this work are based on the Si/SiGe system. Their layout is given in Figure 3.14 (a). The epistructure of the MODFETs is as follows: first, a thick (3□m) relaxed linearly graded SiGe virtual substrate was grown over a p-doped conventional Si wafer. The final top Ge molar fraction in the virtual substrate was 0.3. The structure has an undoped 12 nm tensile strained Si channel sandwiched between two n-doped $Si_{0.70}Ge_{0.30}$ relaxed supply layers (reddish layers) to generate a high density of electrons in the strained-Si quantum well [52], [53]. The highlighted bluish layer marks out the strained-Si quantum well. Pt/Au were evaporated on a very thin silicon layer to fabricate the Schottky-gate. The gate was not symmetrically placed between source and drain. A more detailed description of the transistor fabrication can be found in [52]. Our strained-Si MODFETs used in this work were fabricated by Thomas Hackbarth (Daimler) and supplied to us by Dr. Kristel Fobelets (Imperial College London).

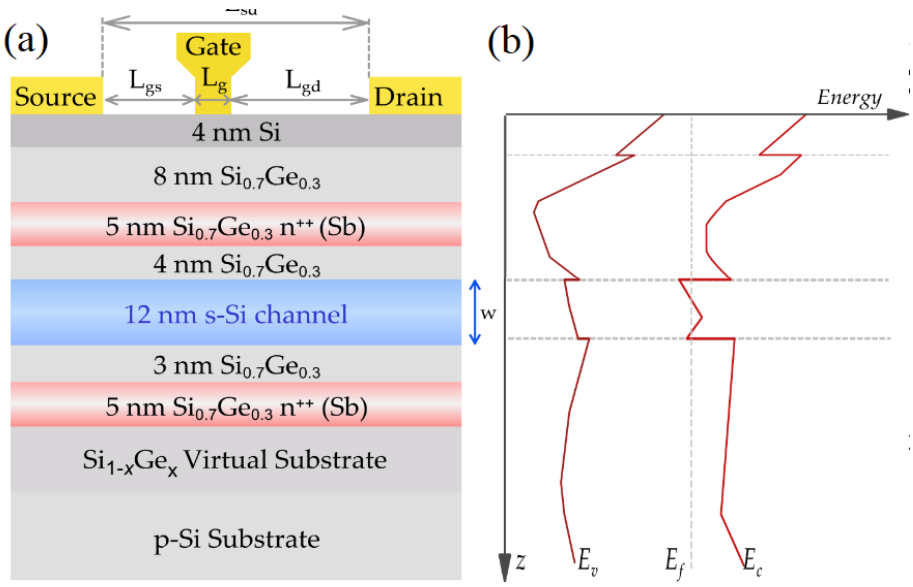


Figure 3.14 (a) Epistructure of the Si/SiGe MODFETs showing the vertical layout of the transistors. (b) Conduction and Valence band profiles and the Fermi level under the gate in equilibrium.

As we showed above, the material system Si/SiGe allows the creation of a biaxial tensile straind layer of silicon on a relaxed SiGe virtual substrate that may be capitalized to fabricate strained–Si n-channel FETs with a theoretical enhancement of the channel electron mobility by a factor nearly two when using values of the Ge molar fraction in the substrate in excess of 0.3 [54], [55]. High-electron mobility FETs (HEMTs), also known as Heterostructure FETs (HFETs) or Modulation-Doped FETs (MODFETs), have been recognized as one of the more suitable candidates to develop soild-state sources and detectors of sub-THz and THz detectors [19]. Si/SiGe HEMTs exhibit competitive advantages as compared to other FETs technologies: Si MOSFETs lack of a high-mobility channel and III-V HEMTs lack of substrate compatibility with Si wafers and, additionally, it is well known that they commonly lead to extensive reliability concerns.

From the above it follows that tensile strained silicon channels will allow us to build high-mobility FETs that will be excellent candidates to detect and generate THz radiation. A vertical cut of the energy band diagram of an unbiased typical Schottky-gate strained-Si/SiGe is given in Figure 3.14 (b). The value of the conduction band offset of the heterojunction $Si/Si_{0.70}Ge_{0.30}$ is about 180 meV according to literature [56] that would ensure an excellent electron confinement in the strained-Si quantum well, necessary for room temperature high-mobility operation of the transistor. The results presented in this work are based on this epilayer. Table 3.2 summarizes the geometrical parameters of the strained-Si MODFETs that were studied.

	L_{DS} (µm)	L_{GS} (µm)	L_G (nm)	W_G (µm)
Device 1 (D1)	2	1	100	30
Device 2 (D2)	2	1	250	30
Device 3 (D3)	2	1	500	30

Table 3.2 Geometrical and electrical parameters of the strained-Si MODFETs under study.

(a) (b) (c)

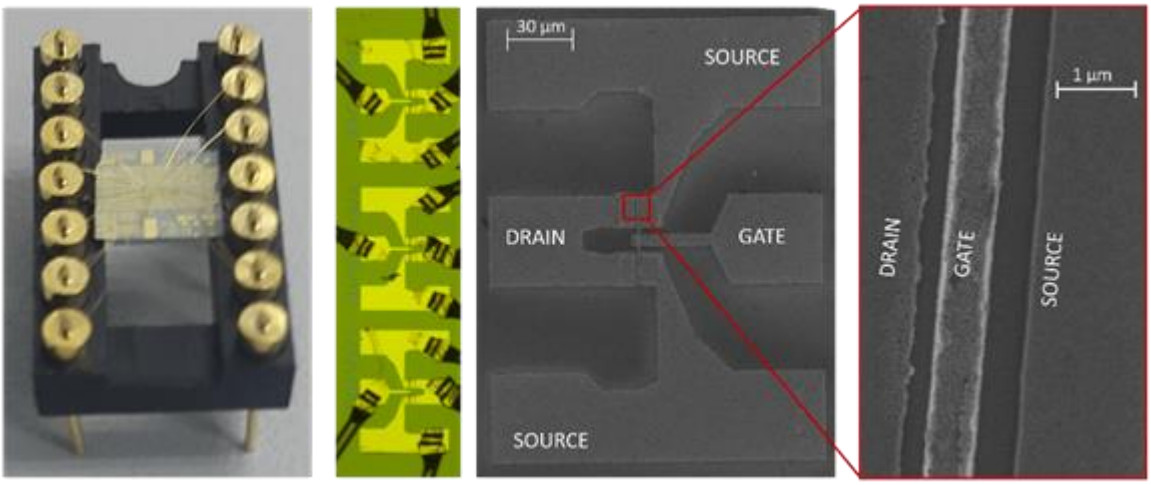


Figure 3.15 Strained-Si MODFETs under study mounted and bounded on a DIP14 (a) and their optical microscope image (b). (c) SEM image of Device 3 (500 nm T-gate transistor).

The channel's length (L_{DS}) and width (W_G) were kept constant for all devices (L_{DS}=2 µm, W_G= 30 µm). However, the gate lengths of the transistors were varied. Transistors with 100-, 250- and 500-nm gate length were characterized. The gates were asymmetrically placed between the source (S) and the drain (D) contacts in all transistors; the distance between the right edge of the source and the left edge of the gate (L_{GS}) was equal to 1µm for all the transistors (Table 3.2). An asymmetrical position of the gate is of interest to enhance THz detection by a transistor [57]. Measuring devices with different values of the gate length allows the study of the influence of the gate length on the performance of the transistors as THz detectors and on the coupling of the incoming THz radiation to the device channel. Strained-Si MODFETs with different gate lengths were mounted and wire-bonded on the same dual in-line package (DIP14) showed in (Figure 3.15 (a)). An optical microscope image of the three different devices under study is given in Figure 3.15 (b). A SEM image of D3 with L_G=500 nm is shown in Figure 3.15 (c).

3.3.3 TCAD modelling

Dyakonov and Shur obtained an analytical solution of the unidimensional Euler equation that demonstrated the ability of plasma-waves developed in FET channels to generate and detect THz radiation [18], [19]. Nevertheless, a single equation cannot account for all the technologically relevant parameters (such as doping profiles, high electric fields that locally modify the carrier mobility, device geometry, etc.) that condition the performance of a FET as a THz detector. Thus, a deeper study is necessary for that purpose. This work presents a theoretical study based on Technology Computer-Aided Design (TCAD) simulations to investigate the transistor response to THz radiation excitation. Two-dimensional (2D) TCAD simulations were validated through comparison with both DC and THz measurements.

3.3.3.1 Basic equations

This section summarizes the most important physical models used in the simulations of the strained- Si MODFETs. An, insufficient, first description of the charge transport in a transistor may be achieved through the numerical solution of the drift-diffusion model (DDM) coupled to a Poisson equation solver (Equation (3.6)) and the continuity equations for electrons (Eq. (3.7)) and holes (Eq. (3.8)) [58]:

$$\nabla^2\varphi = -\frac{q}{\varepsilon}\left(p - n + N_D^+ - N_A^-\right) \tag{3.6}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\left(\vec{\nabla}\cdot\overrightarrow{J_n}\right) - U_n \tag{3.7}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\left(\vec{\nabla}\cdot\overrightarrow{J_p}\right) - U_p \tag{3.8}$$

where φ is the electric potential, q is the absolute value of the electron charge, n/p is the electron/hole concentration, N_D^+ $\left(N_A^+\right)$ is the ionized donor (acceptor) concentration, ε is the local material permittivity and U_n $\left(U_p\right)$ represents the net electron (hole) recombination rate. $\vec{J}_n$ $\left(\vec{J}_p\right)$ is the current density of electrons (holes) in the drift-diffusion model given by the equations (3.9) and (3.10):

$$\overrightarrow{J_n} = q\mu_n(u_n)[n\vec{E} + \vec{\nabla}(u_n n)] \tag{3.9}$$

$$\overrightarrow{J_p} = q\mu_p(u_p)[n\vec{E} + \vec{\nabla}(u_p p)] \tag{3.10}$$

where $\vec{E}$ is electric field, μ_n μ_n (μ_p) is the electron (hole) mobility and μ_n (μ_p) is the electron (hole) thermal voltage. In deep-submicron FETs, the drain and gate biases give rise to large electric fields that rapidly change over small length scales giving origin to nonlocal phenomena that will dominate the transistor performance [52], [53]. As carriers are intensely heated by the electric field in the channel of deep-submicrometer FETs energy balance equations accounting for electron and hole heating and energy relaxation in the device must be self-consistently added to the transport model. Since, the DDM only considers moment relaxation [47], it is unable to describe hot carrier transport. As channel mobility is closely dependent on the carrier temperature an extended model needs to be used to study the electric properties of deep-submicron FET transistors used in plasma wave THz detection. This extended model is known as the hydrodynamic model (HDM).

The HDM [47], [59] includes carrier energy balance by coupling to the set of DDM equations (Eqs. (3.6) - (3.8)) and the electron and hole energy flow densities (Eqs. (3.9) - (3.10)) that are given as:

$$\vec{\nabla}\cdot\overrightarrow{S_n} = \frac{1}{q}\overrightarrow{J_n}\cdot\vec{E} - \frac{3}{2}\left(p\frac{u_n - u_0}{\tau_n} + \frac{\partial(u_n n)}{\partial t}\right) \quad \textbf{(3.11)}$$

$$\vec{\nabla}\cdot\overrightarrow{S_p} = \frac{1}{q}\overrightarrow{J_p}\cdot\vec{E} - \frac{3}{2}\left(p\frac{u_p - u_0}{\tau_p} + \frac{\partial(u_p p)}{\partial t}\right) \quad \textbf{(3.12)}$$

where $\overrightarrow{S_n}$ $(\overrightarrow{S_p})$ is the electron (hole) energy relaxation time, u_n (u_p) is the above-referred electron (hole) thermal voltage and the electric field that is self-consistently obtained from the Poisson equation.

Strained-Si MODFET is essentially a majority carrier device, then the hole energy balance equation (Eq. 3.12) was disregarded in our model. In the present work, a two-dimensional HDM for electron transport and DDM for hole transport (Eqs. (3.6) -(3.11)) was used in TCAD simulations. Carrier relaxation times were obtained from uniform-field Monte Carlo simulations [60], [61]. In TCAD simulations impurity de-ionization, Fermi-Dirac statistics and mobility degradation due to both longitudinal and transverse electric field were considered. All TCAD simulations were carried out at room temperature.

3.3.3.2 Mobility models

As we mentioned above, carrier mobility is a key parameter in the semiconductor technology, thus, accurate models are necessary to describe carrier mobility, μ_n and μ_p, in the device. We selected two different models [30]; the first one is a general mobility model for electrons and holes based on the concentration and the second one is a mobility model based on the surface scattering conditioning the mobility in device.

3.3.3.2.1 Concentration model

For simple materials as Si, a concentration- and temperature-dependent empirical mobility model is given by the equations (3.13) and (3.14):

$$\mu_{0n} = MUN.MIN + \frac{MUN.MAX\left(\frac{T}{300}\right)^{NUN} - MUN.MIN}{1 + \left(\frac{T}{300}\right)^{XIN}\left(\left(\frac{N_{total}}{NREFN}\right)^{ALPHAN} + \left(\frac{N_{total}}{NREFN2}\right)^{3}\right)} \quad \textbf{(3.13)}$$

$$\mu_{0p} = MUP.MIN + \frac{MUP.MAX\left(\frac{T}{300}\right)^{NUN} - MUP.MIN}{1 + \left(\frac{T}{300}\right)^{XIP}\left(\left(\frac{N_{total}}{NREFP}\right)^{ALPHAP} + \left(\frac{N_{total}}{NREFP2}\right)^{3}\right)} \quad \textbf{(3.14)}$$

where N_{total} is the local total impurity concentration (in cm^{-3}) and T is temperature (in K). The default values used for silicon are given in Table 3.3:

Parameter	Silicon	Parameter	Silicon
MUN.MIN	55.24	MUP.MIN	49.70
MUN.MAX	1429.23	MUP.MAX	479.37
NrefN	1.072E17	NrefP	1.606E17
NrefN2	1E30	NrefP2	1E30
Nun	-2.3	Nup	-2.2
XIN	-3.8	XIP	-3.7
ALPHAN	0.73	ALPHAP	0.7

Table 3.3 Default silicon parameters on the mobility concentration model

Values showed on Table 3.3 are validated from experimental measurements in bulk Si. As we metioned above, our devices have a strained-Si channel and thus, electron channel mobility is enhanced with respect to bulk Si, so the values showed in Table 3.3 (MUN.MIN and MUN.MAX) were manually ajusted for the channel to obtain channel mobility values similar to the experimental ones. Since the studied devices are n-channel FETs, the values for holes showed on Table 2.3 don´t need a very precise adjust.

A modified version of the previous mobility model is used for compund materials. The mobility model has to be modified to include composition-dependent maximum and minimum mobilities.

$$\mu_{0n}(x,T) = \mu_n^{\min}(x) + \frac{\left[\mu_n^{\max}(x)\cdot\left(\frac{T}{300}\right)^{NUN} - \mu_n^{\min}(x)\right]}{1+\left(\frac{T}{300}\right)^{XIN}\left(\left(\frac{N_{total}}{NREFN}\right)^{ALPHAN} + \left(\frac{N_{total}}{NREFN2}\right)^{3}\right)} \quad \textbf{(3.15)}$$

Where x is the molar fraction of Ge, $N_{total}(x)$ is the local total impurity concentration and $\mu_n^{min}(x)$ and $\mu_n^{max}(x)$ are, respectively, the minimum and maximum electron mobilities defined according to Equations (2.16) and (2.17) respectively :

$$\mu_n^{\min}(x) = x\cdot MUN.MIN1 + (1-x)\cdot MUN.MIN0 - x(1-x)\cdot MUN.MIN2 \quad \textbf{(3.16)}$$

$$\mu_n^{\max}(x) = x\cdot MUN.MAX1 + (1-x)\cdot MUN.MAX0 - x(1-x)\cdot MUN.MAX2 \quad \textbf{(3.17)}$$

Parameters MUN.MIN0 and MUN.MIN1 are the minimum electron mobilities in ($cm^2/(V\cdot s)$) for x=0 (i.e. Si) and x=1 (ie. Ge), respectively. Similarly, MUN.MAX0 and MUN.MAX1 are the maximum values of electron mobilities for x=0 and x=1 respectively. MUN.MIN2 and MUN.MAX 2 are the corresponding bowing parameters. These parameters must be properly fitted to obtain theoretical values comparable to the experimental ones obtained on bulk SiGe (Figure 3.11). An analogous form (p instead of n) of this model is used for holes.

3.3.3.2.2 Surface scattering model

Along semiconductor interfaces, carrier mobilities can be substantially lower than in bulk semiconductors due to the scattering mechanisms on the surfaces (roughness, charges, etc.). Since the devices studied on this work are based on strained-Si, a specific model for biaxially strained silicon is used (Roldan´s model) [30]. This model combines models for phonon scattering, surface roughness scattering, and screened Coulomb scattering in terms of the $Si_{1-x}Ge_x$ substrate molefraction x. The model parameters have been calibrated at 300K; no explicit temperature dependence was considered.

Using Mathiessien's rule, the total low field mobility is calculated according to equation 3.18:

$$\frac{1}{\mu_s} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_C} \tag{3.18}$$

where μ_{ph} is the phonon-limited mobility, μ_{sr} is the surface roughness limited mobility and μ_C is the Coulomb scattering-limited mobility. These mobilities are given by equations (3.19) - (3.21):

$$\frac{1}{\mu_{ph}} = \frac{1}{MUPH0 \cdot \beta(x)} \left[1 + \left(\frac{E_\perp}{E0} \right)^{0.2 \cdot \alpha(x)} \right] \tag{3.19}$$

$$\frac{1}{\mu_{sr}} = \frac{E_\perp^{\ 2}}{\delta(x) \cdot 1E14} \tag{3.20}$$

$$\mu_C = \max(\mu_{sc}, \mu_b) \tag{3.21}$$

where $E_\perp$ is the component of the electric field normal to the surface, (that is responsible for a large degradation of carrier mobility in MOSFETs, in HFETs this degradation is mitigated due to the better quality of the heterojunction between two semiconductors as compared to the one between silicon and silicon oxide in a MOSFET). μ_b is the bulk mobility given by the mobility model described in section 3.3.3.2.1 "Concentration Dependent Mobility" and μ_{sc} is the screened Coulomb mobility given by:

$$\frac{1}{\mu_{sc}} = c \cdot \frac{N_{tot}}{n} \tag{3.22}$$

where N_{tot} is the total doping concentration and n is the carrier concentration. The fitting functions, α(x), β(x), δ(x) are all dependent on the substrate mole fraction and are given in the next equations:

$$\alpha(x) = 1 + \frac{Aalpha \cdot X}{\left[1 + \left(\frac{Aalpha \cdot X}{0.9} \right)^{Balpha - 1/Balpha} \right]} \tag{3.23}$$

$$\beta(x) = 1 + \frac{Abeta \cdot X}{\left[1 + \left(\frac{Abeta \cdot X}{2.7} \right)^{Bbeta - 1/Bbeta} \right]} \tag{3.24}$$

$$\delta(x) = delta0 + \frac{Adelta \cdot X}{\left[1 + \left(\frac{Adelta \cdot X}{Delta}\right)^{Bdelta-1/Bdelta}\right]} \quad \textbf{(3.25)}$$

3.3.3.3 Transient simulations

As we mentioned in Chapter 1, M. Dyakonov and M. Shur predicted in their pioneering work the detection of the THz using FETs. They proposed a photovoltaic-mode detection with an open-circuit drain FET that was gate-to-source biased and subjected to an electromagnetic radiation. Under these conditions a DC drain-to-source voltage is developed that transduces the THz radiation power. Since the TCAD simulator used lacks of a Maxwell solver we conducted simulations superimposing a small sinusoidal signal to the gate bias (with the desired frequency in the THz range) while the source was kept grounded and the drain was kept floating as it is done in measurements (photovoltaic-mode). The amplitude signal of the sinusoidal wave was fixed to an arbitrary value of 5 mV. Since this value is arbitrary, the magnitude of the THz response obtained in simulations will be presented henceforward in the figures as arbitrary magnitude. As the sinusoidal wave is a continuous wave of of time (t), HDM equations (Eqs. (3.6) - (3.11)) must be solved in the time domain to obtain the voltage generated on the drain contact and then calculate the device photoresponse. All transient simulations were performed by imposing an adequate small step time (t_k). Moreover, the voltage generated on the drain contact by the THz radiation will also exhibit an oscillating behavior. An adequate number of periods must be simulated to obtain a stable solution since the photoresponse generated by the imposed THz radiation is defined as the time-averaged potential created on the drain contact while the source is grounded [19].

3.3.4 Results and discussion

In this section we will show the results obtained from both simulations and experimental measurements.

3.3.4.1 Preliminary results

As a starting point, to ensure precise results obtained from TCAD simulations, it is necessary to properly define the device structure on the 2D TCAD environment and create an adequate meshing to ensure an accurate numerical solution of the model equations described in section 3.3.3. The geometry and dimensions used in the simulations were the ones given in section 3.3.2. The doping level of the supply layers (as opposed to conventional MODFETs the one under study has two supply layers –one above and another one bellow the strained channel to ensure a high concentration of carriers above threshold) was 10^{19} cm^{-3} for the upper supply layer and $1.8 \cdot 10^{18}$ cm^{-3} for the lower one. A uniform residual n-type doping density of 10^{15} cm^{-3} was assumed in the non-intentionally doped regions of the transistor (see Figure 3.16 (b)). The thickness of the virtual substrate and the p-Si wafer were chosen to be 600 nm and 500 nm respectively, to economize computer memory. Under both source and drain contacts highly-doped regions were considered, ensuring low values of the contact resistance of

these ohmic contacts. The value of the conduction and valence bands offsets between the strained-Si and the relaxed $Si_{1-x}Ge_x$ for a Ge molar fraction x=0.30 were extracted according to the theoretical calculations showed in section 3.1 [38]. Low electric field mobility in the channel was modeled using the Roldan's model for biaxially-strained Si on relaxed SiGe as it was described in section 3.3.3.2.2 where the maximum value of th electron mobility in the channel was fixed to 1,600 $cm^2/(Vs)$ [38].

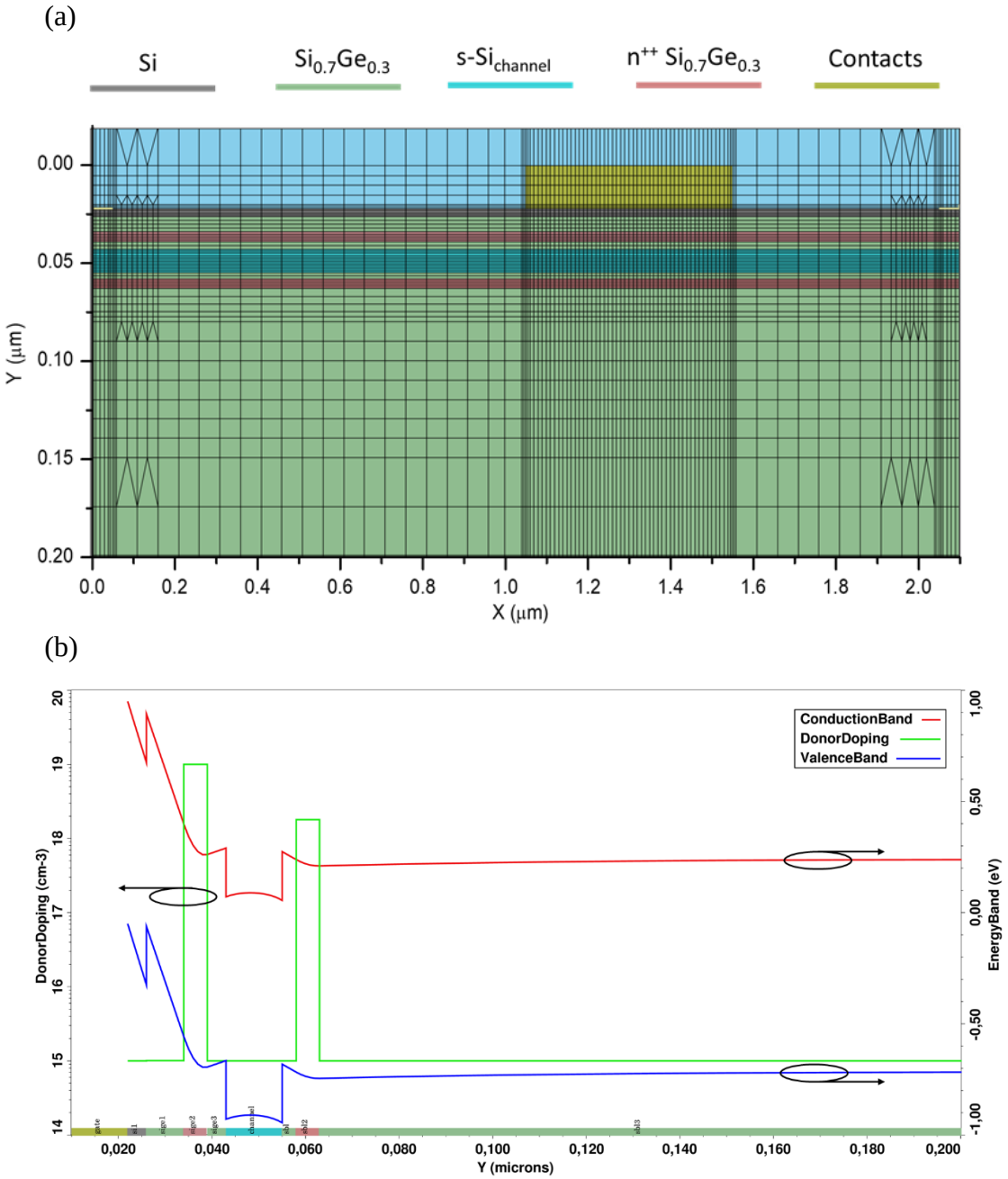


Figure 3.16 Meshing (a) and Conduction and Valence Energy bands and Donor dopping (b) for the Device 3.

Figure 3.16 (a) shows a zoomed image of the meshing for Device 3 with 500 nm gate length. Meshing is essentially the same for all the devices as the only distinguishing parameter between the three devices is the gate length. Since the main region of the device is located on the upper part of the device, a refined meshing was performed on the strained-Si channel, the two n-doped $Si_{0.70}Ge_{0.30}$ relaxed supply layers and the adjacent

layers. Away from the active region the meshing size becomes progressively larger - this is justified by the scarce spatial variation of the electric potential out of the active region of the transistor - till the p-doped Silicon substrate located at the bottom side of the device. The energy band diagram extracted from TCAD simulations under the gate contact at zero voltage is presented in Figure 3.16 (b). The value of the conduction band offset of the heterojunction $Si/Si_{0.70}Ge_{0.30}$ was taken as 180 meV according to literature. This value ensures, as discussed above, an excellent electron confinement in the strained-Si quantum well layer that is necessary for room temperature high-mobility operation of the transistor.

3.3.4.2 DC characterization

Transfer characteristics of Device 3 are given in Figure 3.17 (a) for two different values, 20 and 200 mV, of the drain-to-source voltage (V_{DS}). The three transistors are depletion-mode devices, so a negative bias voltage must be applied to the gate (i.e. a negative gate-to-source voltage) to cut-off the channel [62], [63]. Transfer characteristics in log-scale show that a total switch-off of the device was not possible and a constant level of drain current (I_{DS}) persists for a gate bias of -1V (8µA for V_{ds}=20mV and 80µA for V_{ds}=200mV). As the drain voltage is moderately raised from 20mV to 200mV the above described behavior is enhanced and the sub-threshold current at V_{GS}=-1V increases when V_{DS} increases. This behavior reveals a moderate control of the channel by the gate electrode due to the double supply-layer that is detrimental for the device performance, in return, as above pointed out, this double deck ensures a suitable concentration of the electron plasma in the channel that is of paramount importance to achieve a good performance of the transistor in THz detection.

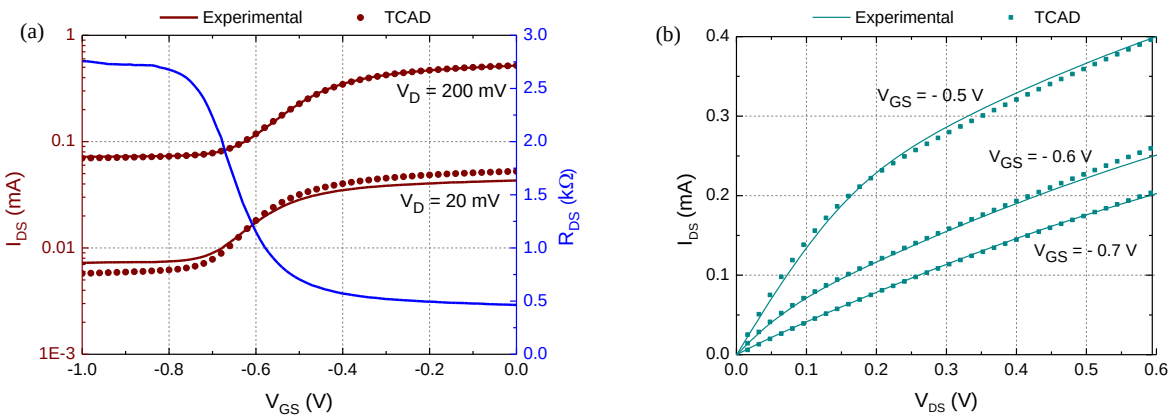


Figure 3.17 (a) Experimental and simulated transfer characteristics on the left axis for Device 3 for two values of the drain voltage plotted in log scale and the device resistance on the right axis as function of the Gate-to-source voltage and (b) output characteristics for three different values of V_{GS}.

The TCAD simulation model of the transistor was validated through comparison with DC and AC measurements. The agreement between TCAD and experimental results across the whole ranges of gate-to-source and drain-to-source biases studied is excellent as Figure 3.17 shows. The extracted values of the threshold voltage (V_{th}) for the transistors are given in Table 3.4; similar values were obtained using TCAD and measurements.:

	Experimental		TCAD	
	V_{th} (V)	g_m/I_{DS} (V^{-1})	V_{th} (V)	g_m/I_{DS} (V^{-1})
D1	-0.75	6.75	-0.77	7
D2	-0.67	6.9	-0.65	9
D3	-0.62	7.5	-0.6	8.5

Table 3.4 Threshold voltage and gm/I_{DS} values obtained from experimental measurements and TCAD simulations

Agreement between measurements and simulations magnitudes involving first derivatives of the drain current was also analyzed. In the first place, the efficiency of the transconductance, defined as the ratio of transconductance (g_m) to drain-to-source DC current (I_{DS}), is a key parameter conventionally used to compare the performance of different technologies of transistors. The efficiency of the transconductance is used here, on the one hand, because it clearly shows the operation region of the device and, on the other hand, because the efficiency of the transconductance is linearly dependent on a current derivative and therefore, discrepancies between simulation and experimental results are readily revealed. Figure 3.18 (a) gives the experimental and calculated efficiency of the transconductance versus the gate voltage (V_{GS}) of transistor D3. The maximum value of the efficiency of the transconductance ($<10V^{-1}$), calculated from measurements and obtained from TCAD simulations is significantly lower than the theoretical limit (38 V^{-1}) [64]. Along with the above discussed behavior of the transconductance, efficiency of the transconductance also suggests that an improvement

of the transistor performance may be achieved by an optimization of the layout of the structure.

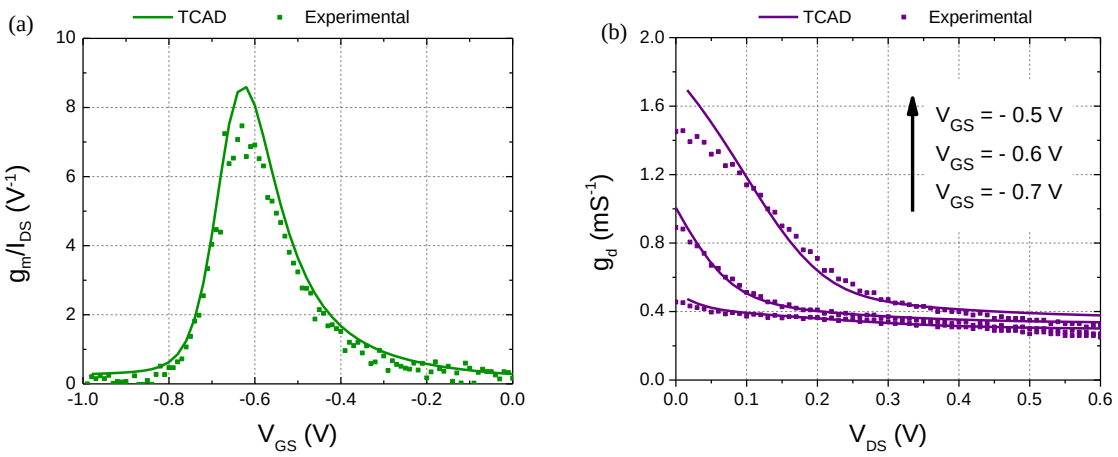


Figure 3.18 (a) Efficiency of the transconductance versus the gate voltage obtained from measurements and numerical TCAD simulations and (b) drain conductance vs. drain voltage for three different values of gate bias obtained from measurements and numerical TCAD simulations.

In the second place, the drain conductance that gives the first derivative of the drain current with respect to the drain current was also determined. Figure 3.18 (b) shows the drain output conductance as a function of the drain voltage at three different gate voltages (-0.5 V, -0.6 V and -0.7 V). Experimental and TCAD drain output conductance curves show, once again, an excellent agreement between measurements and TCAD simulations.

3.3.4.3 THz detection: TCAD vs experimental

As above stated the TCAD study of the THz photovoltaic response of the transistor was implemented, as in measurements, grounding the source, biasing the gate and floating the drain contact while a THz small sinusoidal signal (0.15 or 0.3 THz) with an amplitude fixed to 5mV was superimposed to the gate voltage [18], [19], [65]. As the DC drain voltage in the photovoltaic mode must be supported by a net charge in the drain region, in TCAD simulations a charge boundary condition was implemented at the floating drain contact with a distributed boundary condition over all nodes of the mesh of the drain electrode. The boundary condition is as follows:

$$\oint \vec{D} \cdot \vec{dS} = Q \qquad \textbf{(3. 26)}$$

where $\vec{D}$ is the electric displacement field, Q is the total net charge and the integral is evaluated over the entire surface of the drain electrode. Equation (3.26) forces the potential on the drain (i.e., the photoresponse of the detector) to be adjusted to produce the correct total charge on the electrode.

In simulations it was found that the drain voltage induced by the THz sinusoidal signal (Figure 3.19 (b)) exhibits both the same shape (sinusoidal) and frequency than the AC signal superimposed to the gate bias (Figure 3.19 (a)); this ensures that no frequency conversion takes place in the studied devices.

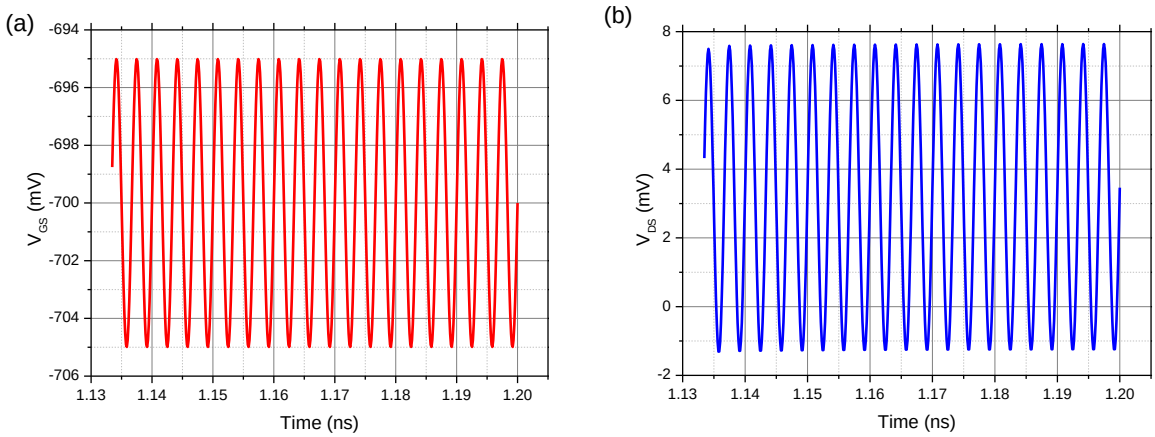


Figure 3.19 0.3 THz imposed (a) and induced (b) signals on the TCAD simulations

Additionally, it was found that its amplitude is smaller (approximately 4mV) than the one of the signal superimposed to the gate in agreement with the fact that in the THz range the transistor is unable to amplify signals and it is merely working as a THz detector (i.e. THz detection is a rectification of the incident THz light). A number of 20 periods was fixed on the TCAD simulations to obtain a stable induced signal on the drain as the initial periods correspond to a transient in the response. The photoresponse obtained in TCAD simulations was extracted, like in measurements, by subtracting the time-averaged drain-to-source voltage when the THz signal was applied $\left(\overline{\Delta U}_{THz-on}\right)$ from the drain-to-source voltage when no signal was applied $\left(\Delta U_{THz-off}\right)$:

$$\Delta U = \overline{\Delta U}_{THz-off} - \Delta U_{THz-on} \qquad \textbf{(3. 27)}$$

Figure 3.20 gives the room temperature photovoltaic response of device D2 with L_G=250 nm obtained experimentally (a) and from TCAD simulations (b) at 0.3 THz (blue squares) and 0.15 THz (red dots).

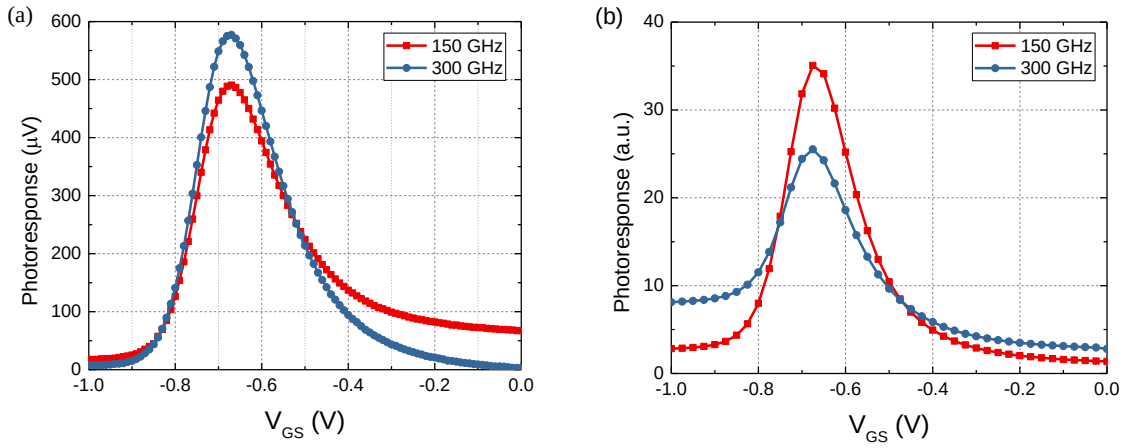


Figure 3.20 Measured (a) and TCAD simulation (b) photoresponse as function of the gate-to-source voltage under excitation of 0.3 THz (blue dots) and 0.15 THz (red squares) of D2.

The higher value of the photoresponse was found when the gate electrode was voltage-biased at a voltage close to the threshold voltage of the transistor [66]. This behavior has been observed earlier in FETs [67], [68] and it was attributed to a non-resonant (broadband) response of the detector since it´s related to overdamping of the plasma waves in the channel where the AC current generated by the incoming radiation at the source cannot reach the drain side of the channel. As we mentioned on Chapter 1, damping or overdamping behavior can be estimated by the dimensionless factor ωτ:

$$\tau = m^* \frac{\mu}{e} \qquad \textbf{(3. 28)}$$

where m^* is the electron effective mass, μ is the electron mobility and e is the absolute value of the electron charge [19]. In the present case, strained-Si MODFETs show higher channel mobility (~1600 $cm^2/V\cdot s$) than conventional Si-MOSFETs (~200 $cm^2/V\cdot s$). The value of the factor described above was estimated to 0.14 at f =0.15 THz and ~ 0.29 at f = 0.3 THz. Both values unfulfill the resonance condition (ωτ>>1).

The experimental photoresponse (Figure 3.20 (a)) is more intense under excitation at 0.3 THz than at 0.15 THz. The photoresponse obtained in TCAD simulations exhibits a behaviour opposite to the observed in device 2: the photoresponse at 0.15 THz is more intense than at 0.3 THz. This must be partly attributed to the fact that in measurements, the source's output power at 0.3 THz is twice the one at 0.15 THz. Moreover, the coupling of the THz radiation to the devices will be different at 0.15 and at 0.3 THz. These possibilities are explored and further discussed below. As in TCAD simulations the amplitude of the sinusoidal gate signal was fixed to 5 mV for both frequencies, no coupling and/or effects related to the differences in the incoming THz power at both frequencies can be found..

THz detection measurements showed on Figure 3.20 were performed modulating the THz beam with a mechanical chopper at 0.33 kHz, then the beam was focused on the device under study nad the generated photovoltage was measured by a lock-in amplifier. The modulation frequency was varied from 0.1 up to 4kHz, but the experimental maximum photoresponse remained unchanged over the whole chopper frequency range 0.1-4 kHz (Figure 3.21). This demonstrates the fast response (0.2 ms or higher) of THz detection using strained-Si MODFETs. Experimental measurements at higher frequency chopper operation were delimited by the slots width of the chopper and the beam diameter since the beam diameter was larger than the slots width.

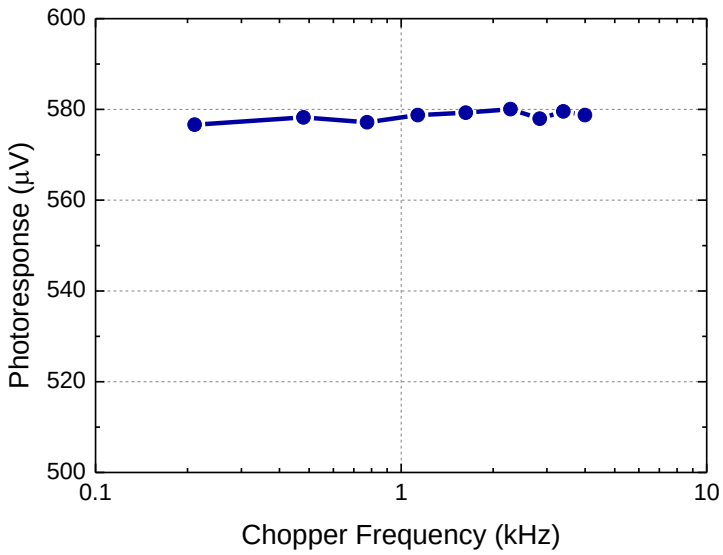
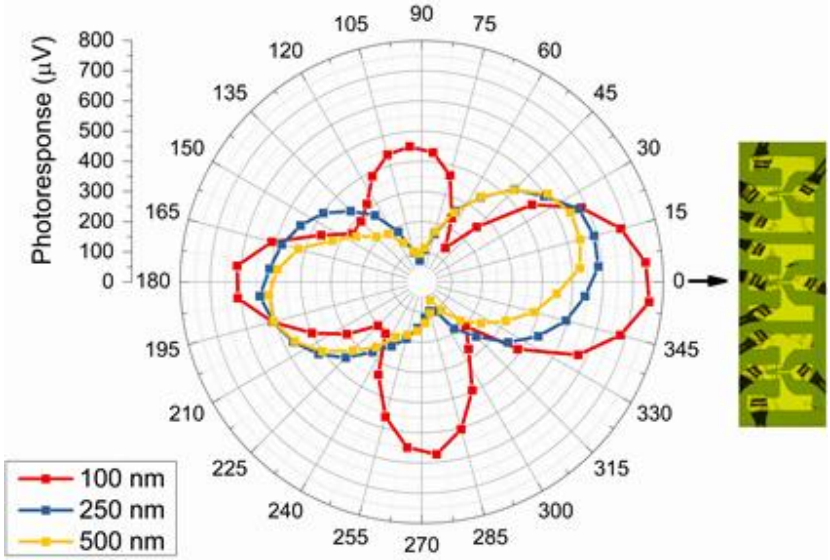


Figure 3.21 Photoresponse at 0.3 THz as function of the chopping frequency for Device 2. The gate voltage was fixed to V_G = -0.67 V.

3.3.4.4 Polarization sensitivity of photoresponse

In Figure 3.20 (a) it was observed that photoresponse is more intense under excitation at 0.3 THz than at 0.15 THz. This must be partly attributed to the higher power at 0.3 THz (~6mW) than at 0.15 THz (~3mW) and to a coupling of the THz radiation to the device that varies with frequency. Moreover, the bonding wires and the metallic pads could play an antenna role to couple the incoming terahertz radiation (linearly polarized) to the 2D electron channel [69]–[71]. To understand how the EM radiation is coupled to the channel, devices were rotated in the plane perpendicular to the terahertz beam and the photoresponse signal was measured for each angular position of the devices under study. Figure 3.22 shows the photoresponse signal as a function of the polarization of the incoming THz radiation for 0.3 THz (a) and 0.15 THz (b).

(a)



(b)

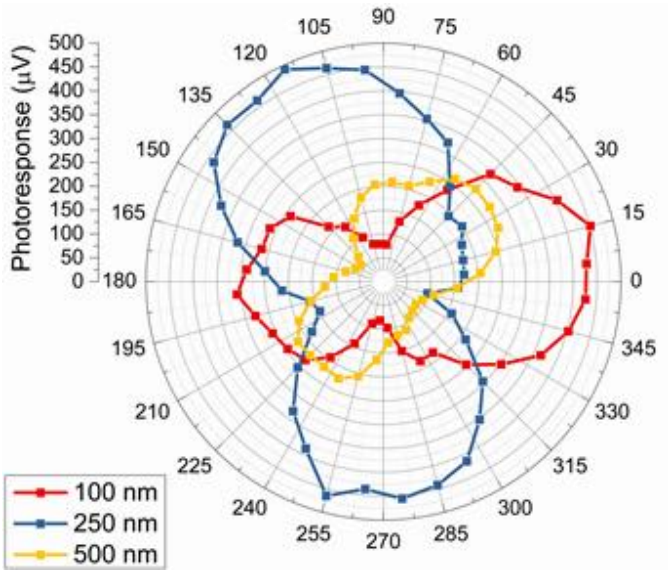


Figure 3.22 Photoresponse vs. rotation angle for all devices under excitation of 0.3 THz (a) and 0.15 THz (b). Inset figure shows the devices at the zero-angle position.

At 0.3 THz all the devices exhibited a maximum of the photoresponse signal when the incoming radiation was parallel to the gate fingers pads (see inset of Figure 3.22 (a)) at zero degrees), showing a maximum photoresponse for all the devices at the same angular position. The maximum photoresponse at 0.15 THz was obtained at different angular positions for each device. This clearly shows that at the lower studied frequency (0.15 THz) bounding wires play an important role to couple the terahertz radiation to the channel of the device. Therefore, at the higher frequency (0.3 THz) the coupling must be mainly performed through the contact pads and/or the gate fingers. These results are in agreement with previously published ones [70].

3.3.4.5 Photoresponse enhancement

Besides the photovoltaic mode, the efficiency of the detector can be improved creating additional asymmetries between drain and source [57], [72], [73]. One method to generate these asymmetries is to apply a DC current between drain and source (I_{DS}>0). Figure 3.23 gives the photoresponse obtained experimentally and from TCAD simulations when a drain-to-source DC current bias, I_{DS} = ±20 µA, is imposed to Device 1 at 0.15 and at 0.3 THz.

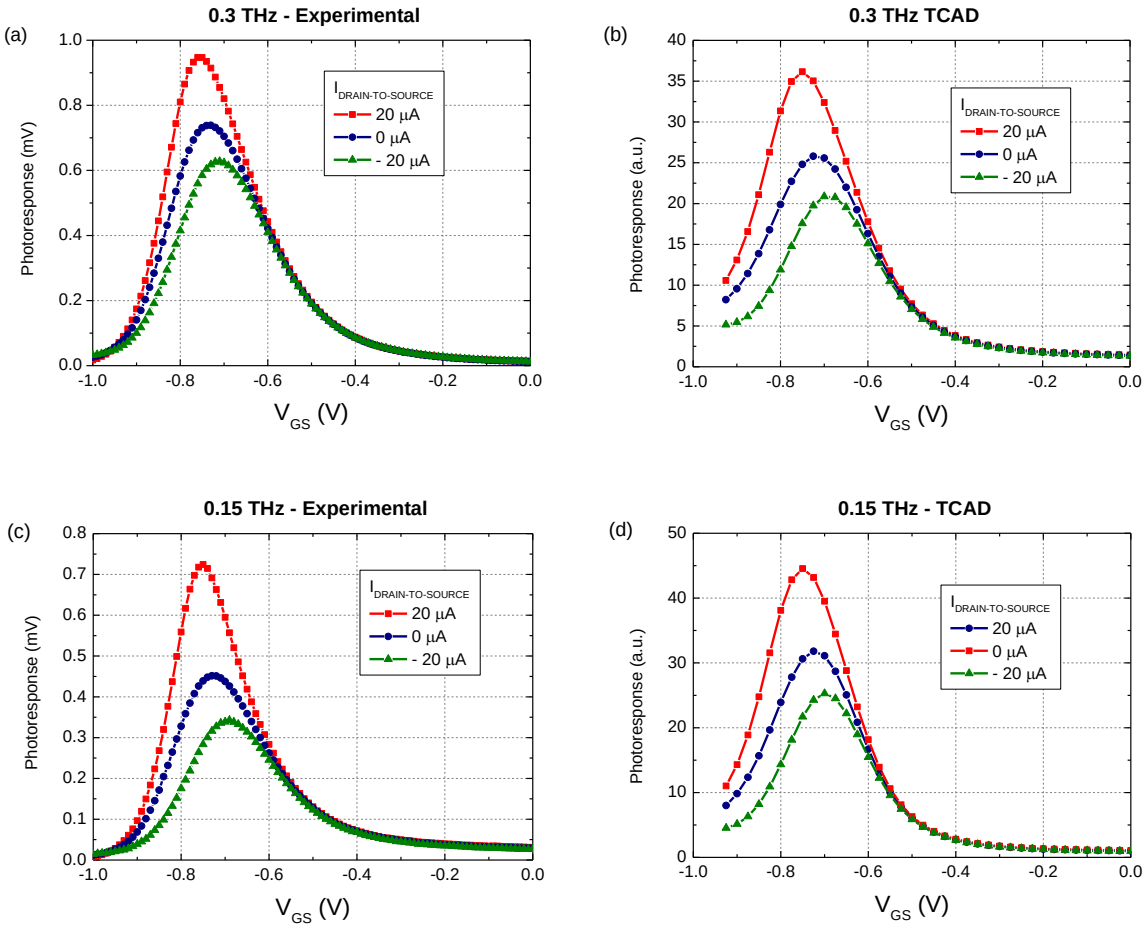


Figure 3.23 Photoresponse vs. gate voltage measured experimentally ((a) and (c)) and obtained from TCAD simulations ((b) and (d)) for different values of I_{DS} at 0.3 and 0.15 THz for D1.

The main effect of imposing a positive DC source-to-drain current bias is that THz detection is significantly enhanced: the photoresponse grows when the bias current is increased. The bias current introduces an additional asymmetry between source and drain, creating a depletion of the electron density on the drain side of the channel and, consequently the maximum value of the photoresponse is also increased [72]–[74]. Contrary, we observed, both experimentally and in TCAD simulations, that imposing a negative drain-to-source DC current the THz detection is worsened. Moreover, a noticeable additional effect is that the maximum of the photoresponse is displaced

towards more negative values of the gate voltage when a positive DC drain current is applied. Figures 3.20 and 3.23 show that the MODFET photoresponse exhibit the same dependence with respect to the gate bias voltage both in measurements and in simulations. An excellent agreement between TCAD and experimental results is found in the photovoltaic mode (I_{DS}=0) and even when a bias current (I_{DS}) is applied to the transistor. Therefore, the measured photoresponse of the strained-Si MODFET must be mainly attributed to the plasmonic response of the channel carriers rather than to the antenna role played by the bonding wires and/or the metal pads as simulations are able to accurately reproduce the experimental photoresponse behaviour.

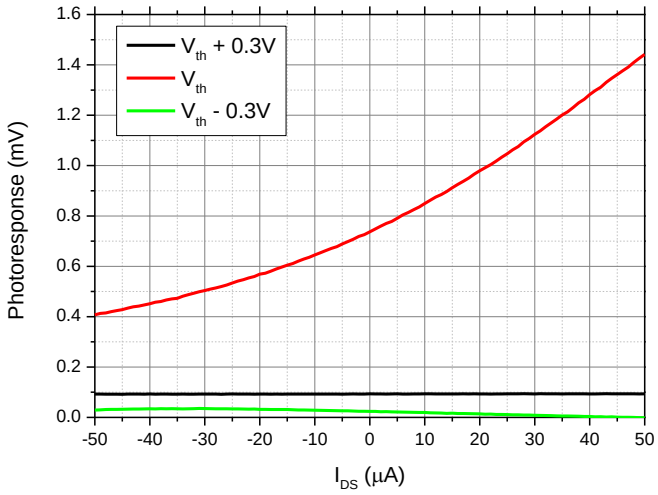


Figure 3.24 Photoresponse vs the drain-to-source current for the Device 2 under different gate-to-source bias

Figure 3.24 shows the photoresponse of Device 2 when a DC drain current is applied. Device photoresponse significantly increases with the applied positive DC drain current (I_{DS}) when the gate is biased at V_{th}. Nevertheless, for values beyond the threshold voltage, the effect of applying a DC current is not observable in the photoresponse. The effect of applying a non-zero DC drain current on terahertz response was first reported by Lu and Shur [72]. They explained that biasing the device by imposing a DC drain-to-source current decreases the value of the gate-to-drain capacitance, while increasing the gate-to-source capacitance, therefore increasing the plasma wave boundary conditions asymmetry, and thus, enhancing the detector response. Moreover, they showed that the photoresponse saturated at a certain drain current saturation current for a given gate bias. When the gate is biased below V_{th} (V_G<Vth) the effect of applying a DC drain current on the device is the lower terahertz response while the value of the DC current necessary to observe the effect becomes higher [72], [75]. Therefore, experimental results showed on Figure 3.24 suggest that we are further away from the saturation regime while the gate is biased at V_{th}. Moreover, when the gate overdrive is possitve (V_{th}+0.3V), the level of the DC I_{DS} current is not enough to produce any improvement of the photoresponse. Finally, we observed that applying a negative I_{DS} current, the photoresponse significantly decreases. Nevertheless, for negative values of the gate overdrive (V_{th}-0.3V), the photocurrent is slightly enhanced by applying a negative I_{DS} current.

	Photoresponse (µV) (IDS = 0 µA)		Photoresponse (µV) (IDS = 50 µA)	
	0.15 THz	0.3 THz	0.15 THz	0.3 THz
D1	457	742	1200	1422
D2	492	580	1693	1635
D3	271	532	543	1053

Table 3.5 Maximum photoresponse values obtained experimentally

Table 3.5 summarizes the maximum value of the experimental photoresponses when the devices were illuminated by 0.15 and 0.3 THz EM radiation while they were either current unbiased or biased with 50 µA drain-to-source current. At the current unbiased conditions, the shorter gate devices show the best performance at 0.3 THz. Nevertheless, when a 50 µA drain-to-source current was applied, the photoresponse of device D2 is greatly enhanced at both frequencies and it exhibits the best performance.

3.3.4.6 Beyond experimental measurements

Additional TCAD simulations were performed to obtain useful information about the THz performance of devices that couldn't be measured because we could not fabricate additional transistors with a redesign of the structure. Since our TCAD model has been experimentally calibrated it can be used as a tool to advance in the study on strained-Si transistors without having recourse to new devices.

3.3.4.6.1 Gate position

As we discussed above, asymmetries created between drain and source greatly improve the efficiency of the detector. Additionally, to the above-mentioned channel asymmetry created by the current bias, a built-in asymmetry can be geometrically introduced by imposing an asymmetric design of the contact pads in the transistor. Figure 3.25 shows the photoresponse obtained from TCAD simulations as a function of the asymmetry factor. The latter is defined as the ratio L_{GS}/L_{GD} where L_{GS} is the distance between the right edge of the source and the left edge of the gate and L_{GD} is the distance between the right edge of the gate and the left edge of the drain (Figure 3.14 (a)). $L_{GS}/L_{GD}=1$ means that the transistor is symmetric. The gate length was kept constant at 500 nm for all the transistors in this study.

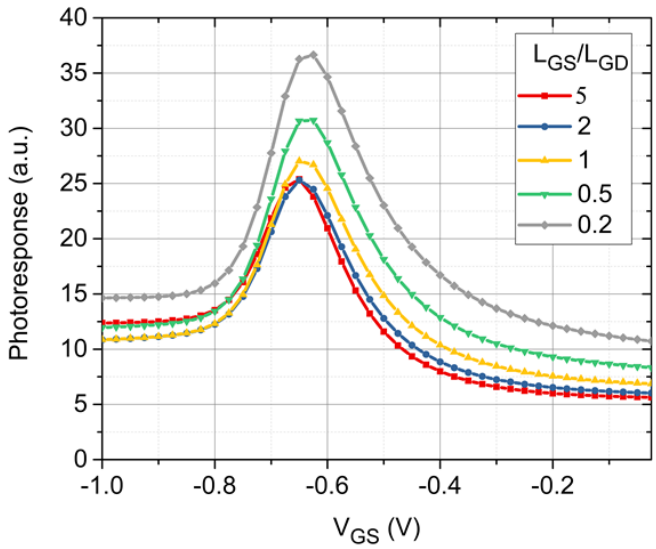


Figure 3.25 Photoresponse obtained from TCAD simulations versus V_{GS} for different horizontal positions of the gate contact.

A higher photoresponse signal was obtained for an asymmetry factor of 0.2 where the gate finger is very close to the source contact. However, in the opposite case, when the gate finger is close to the drain pad, no enhancement of the photoresponse was obtained. In the non-resonant regime, the oscillation of the plasma occurs at a place in the channel very close to the source-channel interface where electrons are injected into the channel and, hence, a gate finger closer to the source pad could efficiently control the damped oscillation of the plasma waves. We may conclude that for a better performance, asymmetry should be introduced as close as possible to the source contact.

3.3.4.6.2 Gate size

An additional design modification can be performed by imposing a different gate size. TCAD simulations at 0.3 THz were performed on the devices while different gate sizes from 50 nm up to 1.5 µm were considered. Gate position was determined by imposing a symmetrical design of the device (i.e. $L_{SG} = L_{GD}$) to ensure that the main contribution to the change of the photoresponse is supported by the gate length modification.

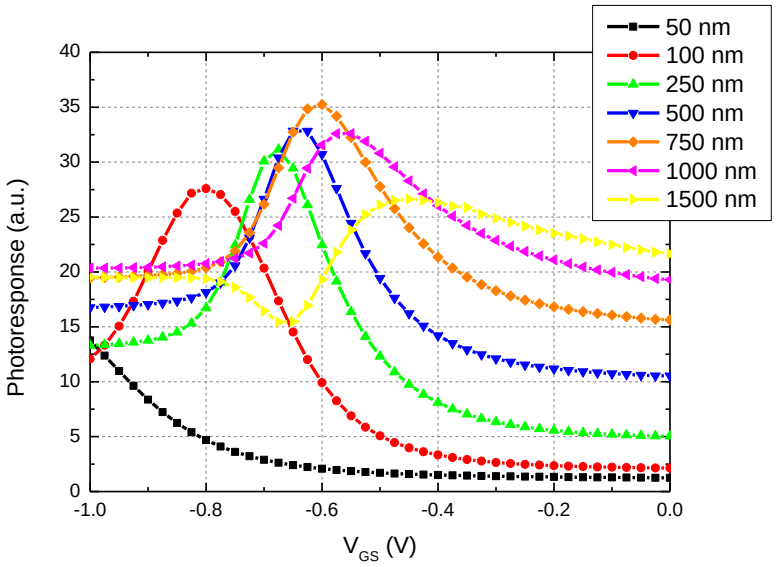


Figure 3.26 Gate length dependence of the photoresponse vs Gate-to-source bias

Figure 3.26 shows the photoresponse obtained from TCAD simulations when a 0.3 THz signal was superimposed to the gate-to-source voltage for different gate lengths. Simulation results shows a clear dependence on the photoresponse when the gate length is modified. A maximum photoresponse was found for a gate length of 750 nm. The smaller gate lengths shows that the maximum photoresponse is reached for more negative gate-to-source voltages, in agreement with a worst control of the channel and the displacement of the threshold voltage to negative values. On the contrary, for the longer gate lengths the maximum photoresponse is obtained for smaller gate-to-source voltages

3.3.4.6.3 Frequency dependence

Finally, the lack of sources on the THz range (THz GAP) makes conducting experimental studies difficult and very expensive, while, TCAD simulations can be easily performed and they are trustworthy enough when predicting the THz detection by transistors.

Frequency-dependence simulations were performed keeping a constant gate-to-source bias close to the threshold voltage of the transistor and varying the signal frequency.

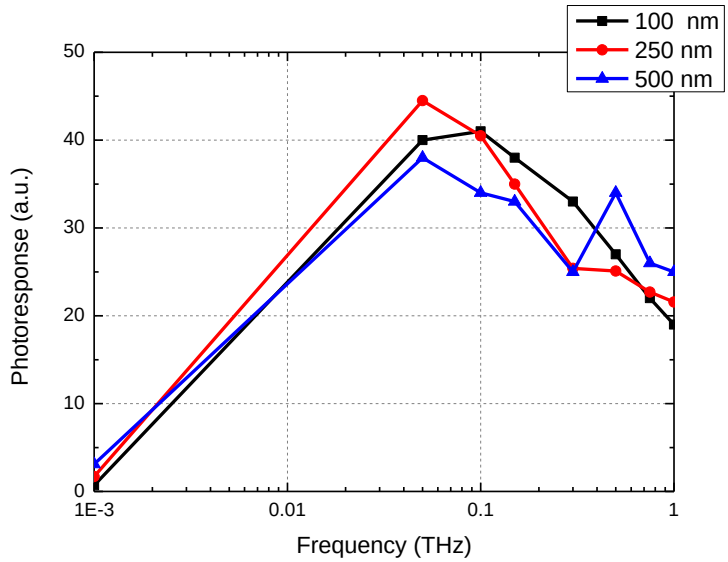


Figure 3.27 Frequency dependence of the photoresponse for the devices under studio

Figure 3.27 shows the photoresponse signal for the three different devices under study when the frequency of the THz signal was varied from 1 GHz up to 1 THz. TCAD simulations showed a similar behavior at 0.3 THz than the one obtained in measurements (Figure 3.22). The maximum photovoltage was produced in the device with the shorter gate length (D1) and the minimum photovoltage was obtained in the device with the longer gate (D3). TCAD simulations show that devices with shorter gates would reach their maxima photoresponse values at higher frequencies than devices with longer gates.

3.3.4.7 Imaging at 0.3 THz

To test the ability of strained-Si MODFETs as detectors of THz radiation, a single transistor (D1) was used as the sensor in the terahertz imaging system described on section 2.2. Figure 3.28 shows the visible image of a standard 8-bit CMOS static shift register (left) and its terahertz image at 0.3 THz (right) when it was hidden inside an envelope. THz radiation passes through in the regions free of metal. A pixel-by-pixel image with a X-Y step of 0.2 mm was taken using D1 as THz detector; the gate of the transistor was biased around its threshold voltage to obtain a maximum intensity of the signal according to the previous experimental measurements. A clear terahertz image was obtained as the internal conections of the chip are observed in Figure 3.28 (b). This THz image confirms the suitability of strained-Si MODFETs as THz detectors for Thz imaging. Obviously, abtter resolution can be obtained using a THz source at a higher frequency owing to its lower wavelength (λ<1mm) than the one used in our experiment.

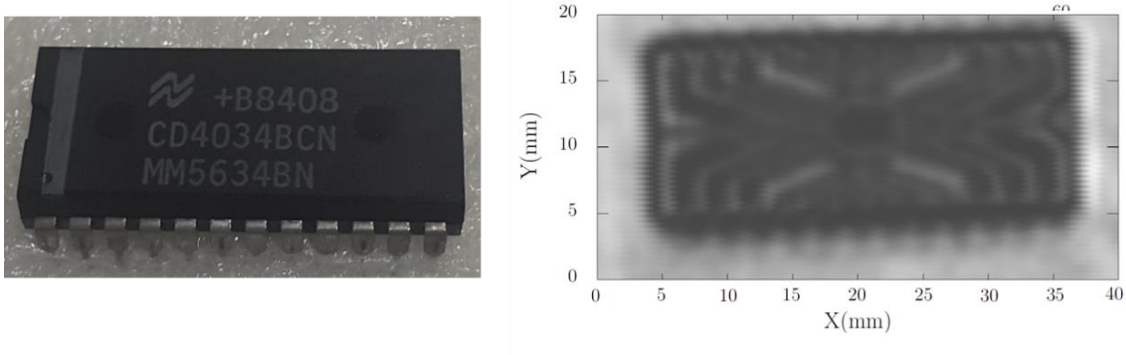


Figure 3.28 Visible (Left) and 0.3 THz (Right) images obtained at room temperature using as sensor the strained-Si MODFET with shorter gate.

3.3.4.8 Responsivity and NEP

Responsivity (R_V) and Noise Equivalent Power (NEP) are the two key parameters (figures of merit) that determine the performance of THz detectors. Responsivity is calculated according to equation (3.29):

$$R_V = \frac{\Delta U S_t}{P_t S_a} \frac{\pi}{\sqrt{2}} \qquad \textbf{(3. 29)}$$

$$NEP = \frac{N_{th}}{R_v} \qquad \textbf{(3. 30)}$$

where ΔU is the photoresponse signal measured with the lock-in amplifier, S_t is the radiation beam spot area, S_a the active area of the transistor, and P_t the total incident power surrounding the detector. The radiation beam power and the spot area were measured using a calibrated pyroelectric detector placed at the position of the THz detector (MODFET) in our experimental setup (see section 2.2); the P_t values were P_t = 0.5mW at 0.15 THz and P_t = 1mW at 0.3 THz. The spot area is given by πr^2 where r is the radius of the beam spot (≈ 1.5 mm at 0.3 THz and 3.3 mm at 0.15 THz). The area of each single transistor, including the contact pads, is lower than 0.05mm^2 (Figure 3.15), i.e. much smaller than the diffraction limit area $S_\lambda=\lambda^2/4$. Accordingly, to obtain Rv from equation (3.29) S_a was replaced by S_λ to avoid overestimation of the Rv as well as underestimation of NEP. The factor $\pi/\sqrt{2}$ comes from the Fourier transform of the square-wave modulated THz signal that is detected as a rms value using the lock-in amplifier.

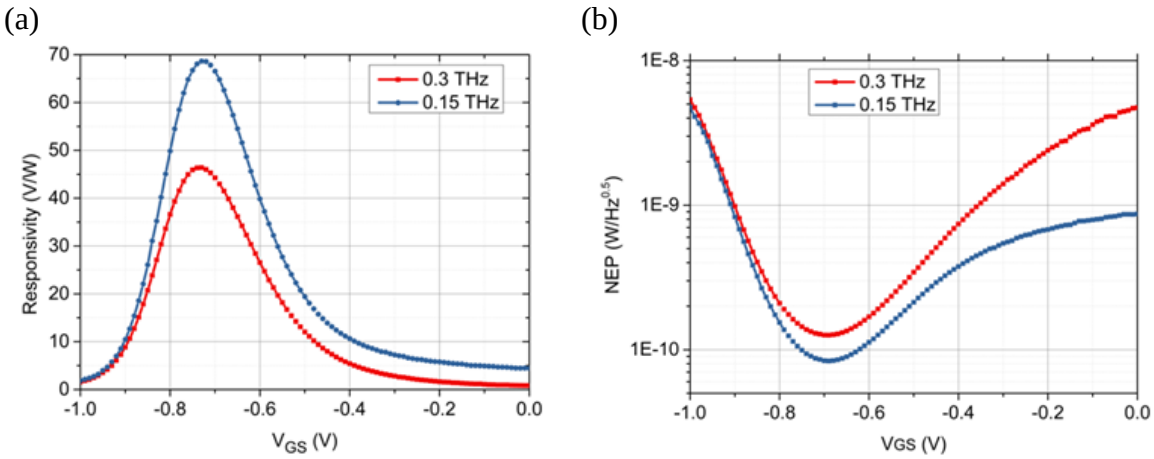


Figure 3.29 Responsivity (a) and NEP (b) measured under excitation of 0.15 THz (blue dots) and 0.3 THz (red squares) of the strained-Si MODFET with 100 nm gate length.

The NEP is given by equation (3.30), where N_{th} is the thermal noise of the transistor in V/Hz$^{0.5}$ and R_V is the responsivity in V/W. Since R_V and the NEP were studied at zero drain current bias, thermal noise $N_{th}=(4kTR_{ds})^{0.5}$, is the only relevant source of noise in the transistor. Here R_{ds} is the drain-to-source resistance that can be extracted from the transfer characteristics measured at low drain-to-source bias (20mV) that corresponds to the linear regime (i.e. Figure 3.17 (a)).

Figure 3.29 presents the responsivity (a) and NEP (b) curves of the device D1 with L_G = 100 nm at 0.15 and 0.3 THz. Table 3.6 summarizes the obtained minimum NEP and maximum R_v for the Si-MODFETs at 0.15 and at 0.3 THz.

	0.15 THz		0.3 THz	
	R_V (V/W)	NEP (nW/$\sqrt{Hz}$)	R_V (V/W)	NEP (nW/$\sqrt{Hz}$)
Device 1	68.6	0.08	46.4	0.12
Device 2	74.5	0.06	36.2	0.13
Device 3	41.1	0.12	33.3	0.14

Table 3.6 Calculated NEPs and R_V for the different devices under studio.

Device 1, with the shorter gate, exhibits the best performance at 0.3 THz with R_V=46.4V/W and NEP ~ 0.12nW/Hz$^{0.5}$ while Device 2 exhibits the best performance at 0.15 THz with R_V=74.5V/W and NEP ~ 0.06nW/Hz$^{0.5}$ This must be, once again, attributed to the large photoresponse signal provided by the Si/SiGe MODFET and to a better coupling of the incoming terahertz radiation at 0.15 THz. The values obtained for the NEP and the responsivity are comparable to the ones of commercial terahertz detectors at room temperature like Golay cells, pyroelectric detectors, and Schottky diodes [76]. However, the Si/SiGe MODFET present the advantage of working at higher modulation frequencies than other detectors.

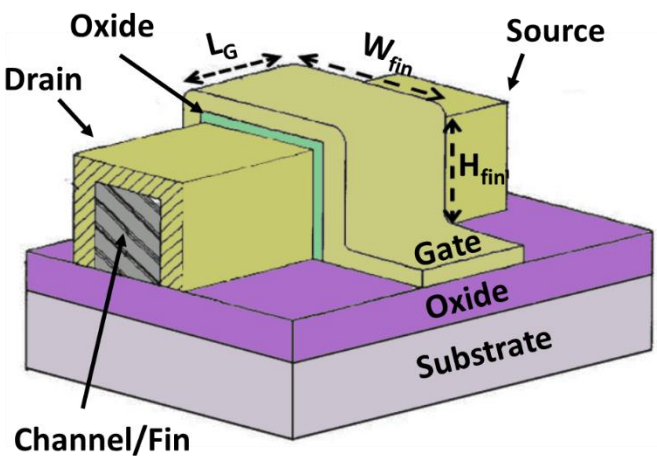
3.4 Silicon FinFETs

3.4.1 Introduction

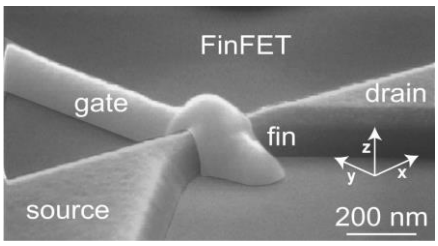
The FinFET concept was proposed in 1998 by Chenming Hu, at that time at University of California at Berkeley, and initially it was named as “Folded Channel Transistor” [77]. The main principle behind the FinFET structure is a thin body, where the gate is placed on two, three, or four sides of the channel or wrapped around the channel so that the gate electrode could be closer to whole channel than in a planar FET. In this way, in FinFETs the gate can effectively control the carrier current in the channel (let us recall our discussion about this issue in the preceding transistors) and, eventually, improving the transconductance of the transistor as compared with conventional bulk CMOS technologies.

Current FinFETs are 3D structures (Figure 3.30 (a) and (b)), also called tri-gate transistors, that can be implemented either on plain silicon or on SOI wafers [78]. The basic FinFET structure consists of a thin (vertical) fin of silicon body on a substrate. The gate is wrapped around the channel providing excellent control from three sides of the channel. The structure is so-called FinFET because its Si body resembles the back fin of a fish.

(a)



(b)



(c)

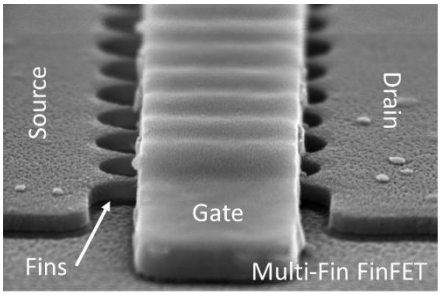


Figure 3.30 Schematic figure of a FinFET () and SEM images of a single FinFET and Multi FinFET [79]–[81]

In bulk-MOS (plannar MOS), the channel is horizontal, while in FinFETs channel is vertical. Therefore, in a FinFET, the height of the channel (Fin Height, H_{fin}) determines the width of the device. The perfect width of the channel ($W_{channel}$) is given by the following equation:

$$W_{channel} = 2H_{fin} + W_{fin} \quad \textbf{(3.31)}$$

The conductive current of a FinFET can be improved by increasing the width of the channel (i.e. by increasing the height of the Fin). Another way to increase the carrier current is based on the construction of parallel multiple fins connected to the drain and source contacts as shown in Figure 3.30 (c).

FinFET technology presents numerous advantages over bulk CMOS, such as higher drive current for a given transistor footprint (hence higher speed), lower leakage (hence lower power consumption) and no random dopant fluctuation (hence better mobility and easier scaling of the transistor beyond 28nm).

3.4.2 Device description

The samples under study in this chapter are based on both n- and p- silicon channel FinFETs. Figure 3.31 (a) shows an optical image of a typical FinFET among the measured during this work. All the studied devices have four independient contacts: Source, Drain, Gate and Bulk. Devices were fabricated by IMEC (Leuven, Belgium). A more detailed description of the fabrication process can be found in [82]. Silicon FinFETs in this chapter are based on the fabrication of multiple fins in parallel. Figure 3.31 (b) shows a TEM image of a FinFETs with 4 Fins in paraller that is similar to the ones studied in this chapter.

The confidentiality agreement with IMEC do not allow us S to give details neither about the fabrication of the FinFETs nor about the geometrical parameter of the devices. Thus, the current work will be focused on the characterization of FinFETs as THz detectors.

(a) (b)

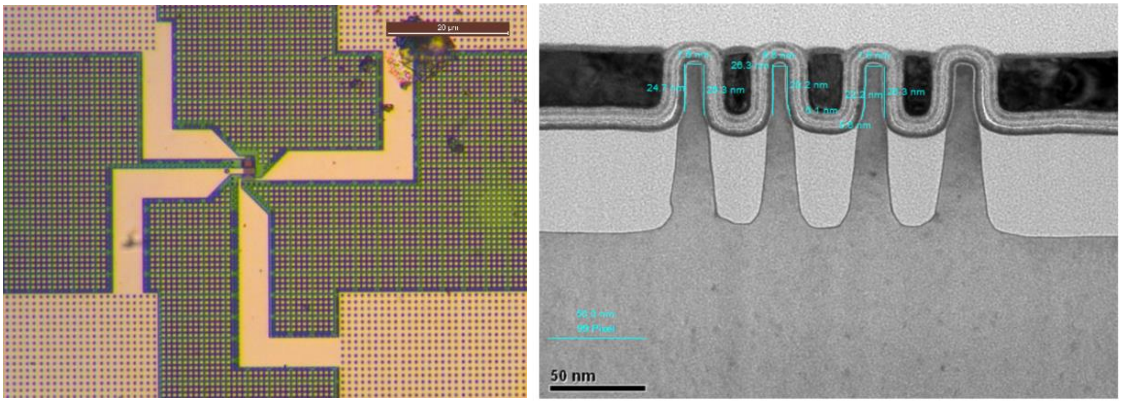


Figure 3.31 Optical image of a typical FinFET device (a) and TEM image of the FinFET with 4 fins (b)

It was shown on section 3.3 the power of TCAD simulations to predict the behavior of strained-Si MODFETs as THz detectors. A similar study could be performed on these silicon FinFETs. Nevertheless, the lack of a detailed knowledge of the internal structure of the FinFETs in this section precluded us from carrying TCAD simulations of this structure.

3.4.3 Results and discussion

3.4.3.1 DC measurements

Transfer characteristics of Device 3 (n-FINFET) and Device 6 (p-FINFET) are shown in Figure 3.32 for two different values, 20 and 200 mV, of the drain-to-source voltage (V_{DS}). Silicon FINFETs are enhancement-mode devices (OFF state at zero gate-to-source voltage) as the technology was developed for CMOS, so a negative (in p-FINFETs) or positive (in n-FINFETs) gate-to-source voltage must be applied to open the channel. A moderate level of current was measured for both p- and n- FINFETs as compared to the previously studied Si/SiGe MOFDETs, in agreement with the reduced device size of the FinFETs. Nevertheless, transfer characteristic in log-scale shows that an excellent switch-off of the device is possible for both p- and n- FINFETs. This indicates an outstandingl control of the channel carrier concentration by the gate.

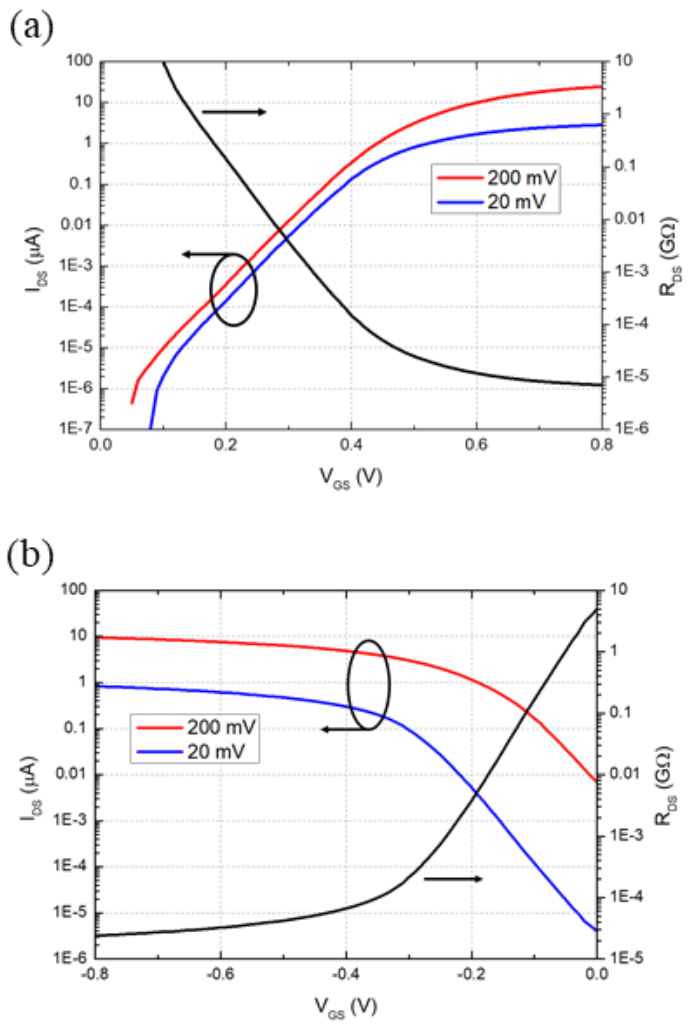


Figure 3.32 Drain-to-source current as function of the Gate Voltage for the device n-FINFET (D3) (a) and p-FINFET (D6) (b)

	V_{th} (V)	g_m/I_{DS} (V^{-1})
Device 1 (D1)	0.32	30
Device 2 (D2)	0.41	34
Device 3 (D3)	0.46	36
Device 4 (D4)	0.37	38
Device 5 (D5)	-0.15	35
Device 6 (D6)	-0.14	35

Table 3.7 Threshold voltage and g_m/I_{DS} values obtained from experimental measurements

Table 3.7 gives the extracted threshold voltage for the FinFETs. A moderate DC voltage on the gate is necessary to open the channel for all the devices, positive values for n-FINFETs and negative values for p-FINFETs. Similarly to section 3.3.4.1, the

magnitudes involving first derivatives of the drain current (g_m/I_D and g_d) were also extracted from measurements.

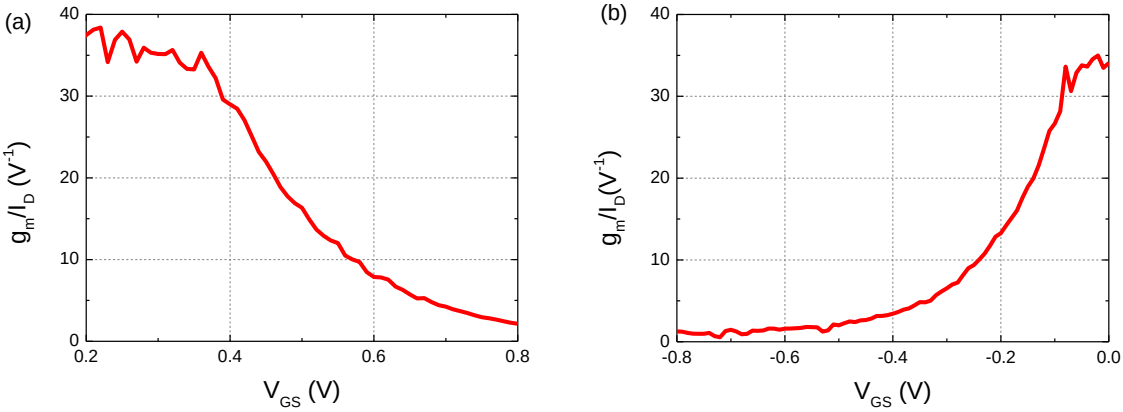


Figure 3.33 g_m/I_D as function of the gate-to-source voltage for the D3 n-FINFET (a) and D6 p-FINFET (b)

Figure 3.33 gives the experimental efficiency of the transconductance (g_m/I_D) versus the gate voltage (V_{GS}) of the devices D3 (a) and D6 (b). The maximum value of the efficiency of the transconductance is close to the theoretical limit at room temperature (38 V^{-1}) for both p- and n- FINFETs. These results suggest that an excellent analog performance may be achieved using the FinFETs, better that the one delivered by the previously studied strained-Si MODFETs.

3.4.3.2 THz measurements

The procedure followed is basically the same as the used in the study of the Si/SiGe MODFETs. But, in this case, FinFEts were THz characterized using the experimental setup showed on Figure 2.3. A continuous THz source was employed to generate THz radiation in the range from 0.14 THz up to 0.44 THz at CEZAMAT. More information can be found in Section 2.3. The devices were biased under the conditions described in section 3.3.4.3, i.e., grounding the source, voltage biasing the gate and floating the drain contact while the THz signal illuminated the transistors.

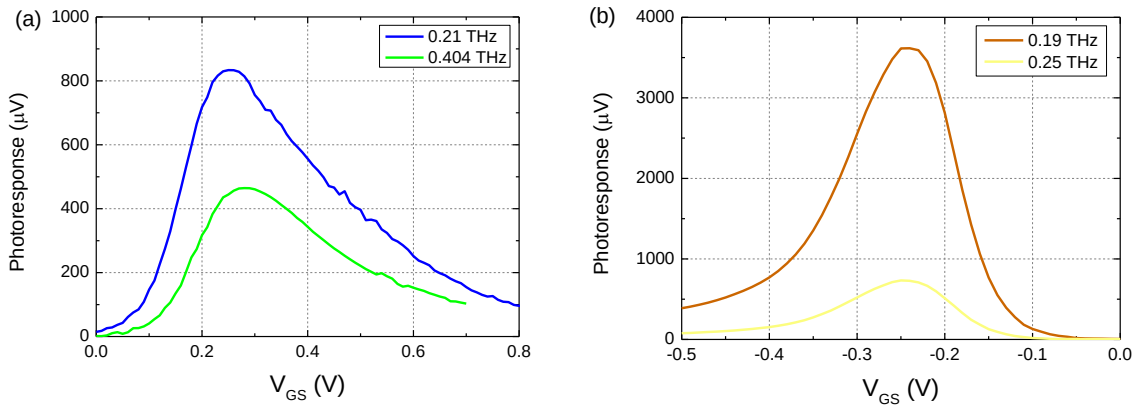


Figure 3.34 Photoresponse as function of the gate voltage at different THz frequencies for the devices D1 n-FinFET (a) and D6 p-FinFET (b)

Figure 3.34 gives the variation of the room temperature photovoltaic response of n-FinFET D1 (a) and p-FINFET D6 (b) versus the gate-to-source bias at two different frequencies. The maximum value in the photoresponse was found, similarly to strained-Si MODFETs (section 3.3), when the gate was biased at a voltage close to the threshold voltage of the transistor. As we mentioned above, the photoresponse behavior is attributed to a non-resonant (broadband) response of the detector related to overdamping of the plasma waves in the transistor channel. Since carrier mobility of the Silicon FinFETs is below 400 $cm^2/V\cdot s$ (~300 $cm^2/V\cdot s$ for n-channel FinFETs and 150 $cm^2/V\cdot s$ for p-channel ones) [82], none of these devices fulfill the resonance condition ($\omega\tau >> 1$), even at the higher frequency range.

A frequency analysis was performance on the FinFETs. The devices were gate-biased at a voltage close to the transistor threshold voltage and keeping the source grounded while the frequency of the THz source was swept 0.14 THz up to 0.44 THz.

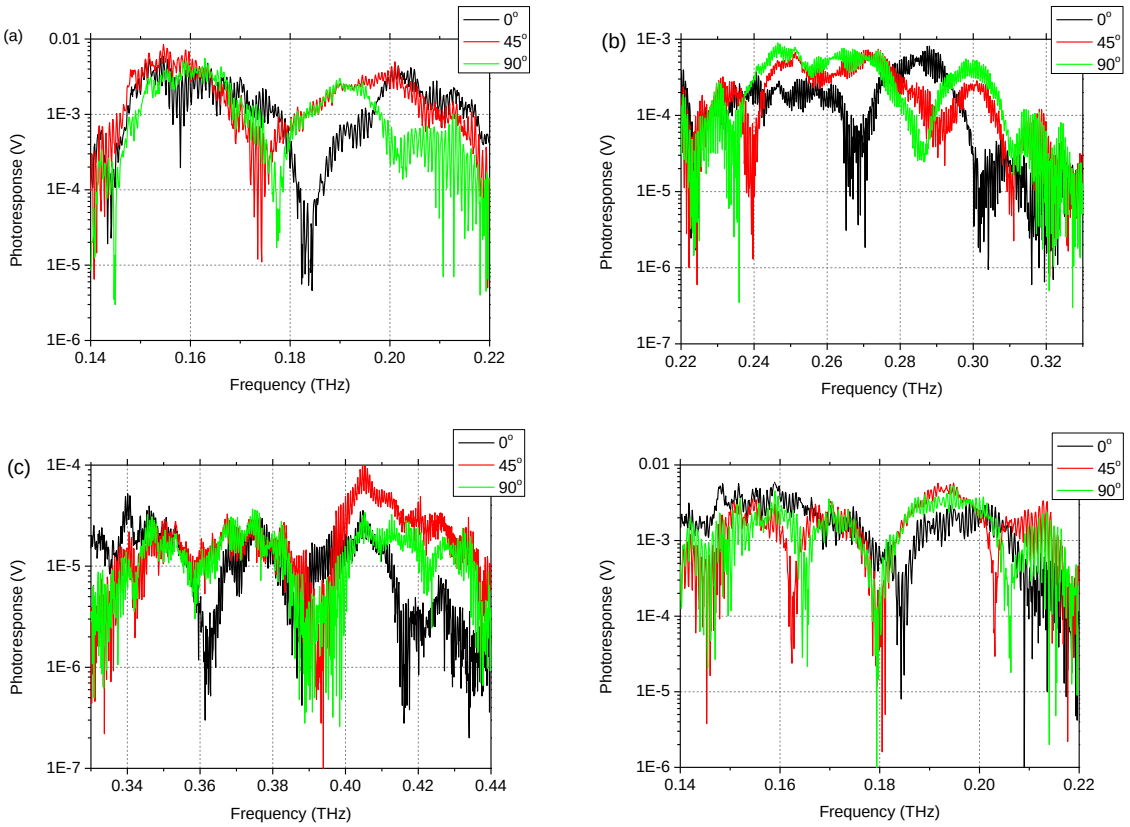


Figure 3.35 Photoresponse as function of the incoming THz frequency at different angle positions for the device D6 (a-c) and the device D1(d)

Figures 3.33 (a)-(c) show the photoresponse when the p-FinFET D6 was illuminated at different frequencies with different polarization angles. It was systematically found on all the characterized devices an oscillating behaviour on the photoresponse while de radiation frequency was varied. Minimum peaks were found across the frequency range that can be attributed to a Fabry-Perot cavity behaviour where the response at some frequencies presents minima [83]. The extinguished frequencies are determined by the cavity whose modes depend on the devices´ structure, layers composition, thickness, etc. Nevertheless, these minimum peaks are strongly affected by the polarization angle of the devices, suggesting that not only the vertical cavity affects the photoresponse, also the pads, fins configuration and position and bonding wires would strongly affect the whole spectral behaviour of the photoresponse. Furthermore, Figure 3.35 (d) shows the photoresponse when the device D1 was radiated by the THz source in the frequency range from 0.14 up to 0.22 THz. A similar behaviour than the one found for the n-channel device was obtained in p-FinFET device D6 when it was rotated and illuminated at different frequencies. Minimum photoresponse peaks were obtained at the same frequencies.

An angle dependence analysis, like the one performed for the strained-Si MODFETs, was also performed on the FinFETs. It was found that at the highest frequencies of the studied range all the devices exhibited a maximum of the photoresponse at the same angle. Four lobes were found on the THz angle measurements at 0.4 THz (Figure 3.36 (a)). Two main lobes were found when the incoming radiation is coupled between the Drain (D) and the

Bulk (B) while the bulk is kept grounded. Top right inset on Figure 3.36 (a) shows the device position when the photoresponse was maximum. Moreover, two additional secondary lobes were obtained when the THz radiation was coupled between the Gate (G) and the Source (S) (Bottom right inset Figure 3.36 (a)).

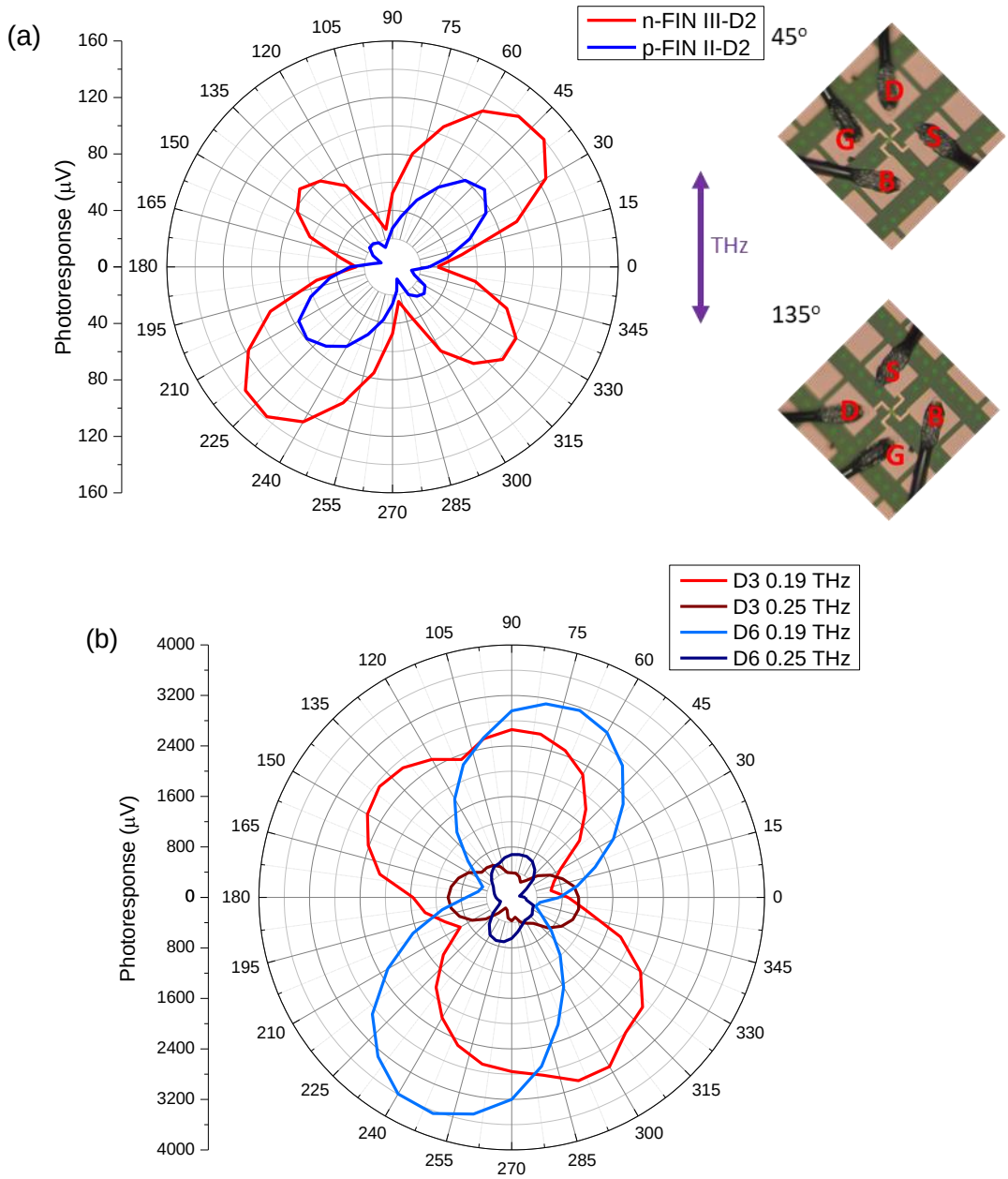


Figure 3.36 Photoresponse as function of the rotation angle for the devices D3 & D6 under excitation of 0.4 THz (a) and 0.25 and 0.19 THz (b). Inset figures shows the devices at the 45° (top) and (135°) bottom.

Nevertheless, at frequencies below 0.25 THz it was found that the behaviour was strongly affected by the bonding wires as the maximum photoresponse was obtained at different angular positions for each device (i.e. Figure 3.36 (b)), like for Si/SiGe devices, this is attributed to the electromagnetic action of the bonding wires.

3.4.3.3 Responsivity and NEP

As we mentioned above, Responsivity and NEP are two key parameters to estimate the performance of any device as detector. Responsivity and NEP were calculated according to the formulas described in section 3.3.4.5, using the diffraction limit area $S_\lambda=\lambda^2/4$ as the area of each single transistor, once again, this procedure will understimate both figures of merit. Figure 3.37 (a) and (b) shows the responsivity and NEP curves for the device III-D2 at 0.19, 0.25 and 0.4 THz versus the gate bias voltage. A maximum value for the responsivity was obtained, as in photoresponse measurements, when the device was gate-biased at a voltage close to the threshold voltage of the device. Similary, the minimum value for the NEP was also obtained for similar biasing conditions.

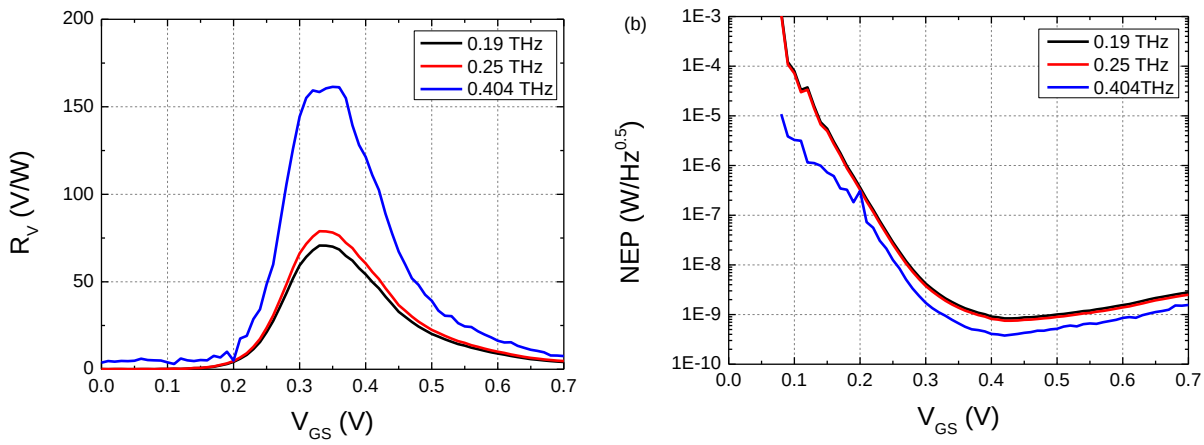


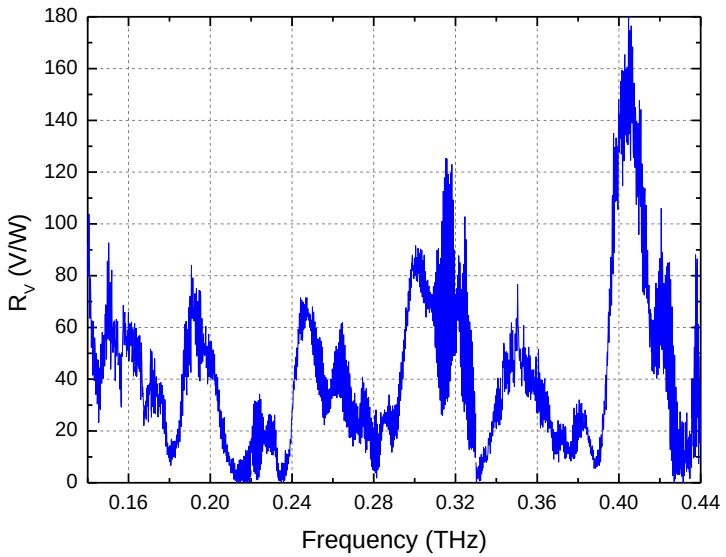
Figure 3.37 Responsivity (a) and NEP (b) as function of the back-gate voltage for the device D3 at 0.19, 0.25 and 0.4 THz

These results clearly show a great performance of FinFETs as THz detectors. At the lower frequencies in the studied range, the magnitude of the FinFET responsivity is similar to the values previously obtained in strained-Si MODFETs because at these frequencies the coupling between the THz radiation and the device is mainly dominated by the bonding wires. In contrast, for higher frequencies, the performance of the Silicon FinFETs compared to the one of strained-Si MODFETs is greatly enhanced since the coupling of the THz radiation is mainly performed by the pads and/or the device. The relatively poorer performance of FinFETs in terms of NEP as compared to Si/SiGe MODFETs is explained by the high channel resistance of the fin (Figure 3.32) as compared with the strained-Si MODFET channel (Figure 3.17 (a)).

Figure 3.38 (a) and (b) shows the responsivity and NEP curves for the device D3 vs the frequency. Values at the lower sub-range of frequencies (<0.28 THz) obtained for the silicon FINFETs are clearly lower than the values obtained from the higher sub-range of

frequencies (>0.28 THz). The above-mentioned oscillating behavior is clearly appreciable on both responsivity and NEP figures from 0.24 THz.

(a)



(b)

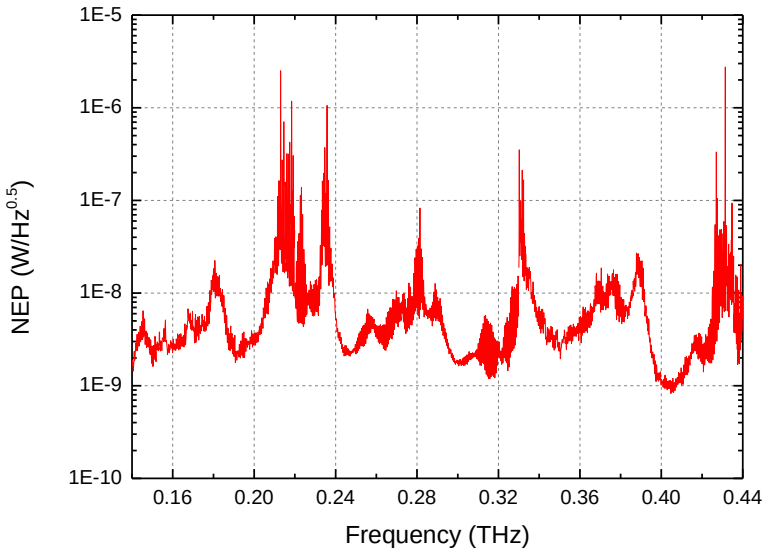


Figure 3.38 Responsivity (a) and NEP (b) as function of the frequency for the device n-FinFET D3

Table 3.8 summarizes the best values obtained for the Responsivity and NEP in our study of FinFETs. Two different ranges were determined to show the performance of the device at low or high frequencies. Beyond 0.275 THz the performance obtained using the n-FINFETs is better than one obtained using p-FINFETs. This could be attributed to a better value of the mobility and effective mass of the electrons on the n-FETs compared with the holes on the p-FETs. Moreover, the best responsivity and NEP values in this

range are obtained at the same frequency radiation close to 0.4 THz. On the contrary, in the low frequency range, the best frequency performance is clearly obtained at different frequencies for every FinFET device. This could be another sign on the role of the bonding wires at low frequencies. Moreover, most of the devices showed a better performance on the high frequency range.

	0.14 - 0.275 THz			0.275 - 0.44 THz		
	R_V (V/W)	NEP (nW/$\sqrt{Hz}$)	f (THz)	R_V (V/W)	NEP (nW/$\sqrt{Hz}$)	f (THz)
D1 LNLA4	70	0.78	@0.225	660	0.05	@0.42
D2 LPLA2	76	2.72	@0.16	103	1.26	@0.407
D3 LPLA4	170	0.63	@0.152	166	1.20	@0.421
D4 LNLA1	123	1.05	@0.193	54	2.11	@0.405
D5 LNLA3	68	2.07	@0.19	161	0.85	@0.406
D6 LNLA4	216	0.33	@0.249	620	0.11	@0.408

Table 3.8 Best values obtained for the Reponsivity and NEP parameters on the THz ranges 0.14-0.275 THz and 0.275-0.44 THz

These devices, both p-channel and n-channel Silicon FinFETs showed an excellent performance in terms of Responsivity and NEP, expecially at high frequency (~0.4 THz). These results suggest that Silicon FinFETs could be efficiently used on real applications such us the one showed in section 3.3.4.7. Nevertheless, the experimental system employed on these study (section 2.3) doesn't allow us to perform such measurements. Additionally, the excellent response at higher frequencies along with an adecuate experimental bench could lead to achive better image resolution as consequence of the higher values of the frequency and thus the smaller beam diameter.

Chapter 4

Graphene FETs

4.1 Introduction

Oscillation of plasma waves into the channel of FET devices was proposed theoretically by Dyakonov & Shur in 1993 [18]. Since then, different experimental demonstrations were achieved using silicon [84] and III-V [85] based devices. Realization of new promising devices for THz detection based on 2D materials was contemplated from 2004, when Geim and Novoselov could isolate a graphene flake and then fabricate the first graphene-based FET [20]. Graphene (as well as other 2D materials) exhibits excellent properties that have attracted interest to develop room-temperature THz sensors and emitters [86] with better performance than silicon technology. Graphene material has demonstrated significant progress in different fields and demonstrated impressive applications; batteries [87], thermal applications [88], membranes for water desalinization [89]... However, controlling the fabrication process of graphene based devices is one of the major challenges to be achieved before it can be considered as a consolidated technology [90]. Graphene in FETs is strongly affected by the substrate and contacting layers degrading their performance. New ideas dealing with the fabrication of graphene-based heterostructures and devices made by mechanical stacking of different 2D crystals on top of each other have emerged in the last years. Detection THz radiation by Graphene-FETs as resonant (frequency selective) [91] as well as non-resonant (broadband) [92] detectors has been studied. However, development of highly efficient detectors and emitters is still under intensive investigations. In this chapter, we´ll describe the fabrication process of new Asymmetric Dual Grating Gate FETs based on graphene heterostructures and their characterization as a future efficient THz device.

4.2 Graphene and Hexagonal Boron Nitride

4.2.1 Graphene

Graphene is described as a single-atom thick layer of carbon atoms with a honeycomb lattice. It was firstly studied theoretically as “2D graphite” by Wallace in 1947 [93]. In 2004 Novoselov and Geim obtained the first graphene monolayer by mechanical exfoliation of bulk graphite. The graphite structure corresponds to a stacking of the hexagonal networks of individual graphene layers in the direction perpendicular to the layer plane (Figure 4.1 (a)). It was believed that 2D materials crystals were thermodynamically unstable and could not exist in the free state [94]. Since then, several new methods were employed to produce graphene: Chemical Vapor Deposition (CVD) method [95], [96], Epitaxial Silicon Carbide (SiC) method [97], [98], Chemical graphene [99], Liquid phase exfoliation of graphite [100] or Electric arc graphene [101], [102]. Nevertheless, mechanical exfoliation method still holds the best quality and performance nowadays.

Since its discovery in 2004, graphene has been the focus of an intense investigation due to its excellent properties. It consists in a sp^2 carbon layered material that has almost the same crystal energy as diamond in which strong covalent bonds are formed between two adjacent carbon atoms (Figure 4.1 (b)). As As each graphene carbon has only three bonds instead of four for diamond, the graphene C–C bonds are about 25% stronger. Thus, it is the strongest material known to date. This property is used to enhance the strength of other materials whish may be useful for different applications: aerospace, building materials, mobile devices, and many others [103].

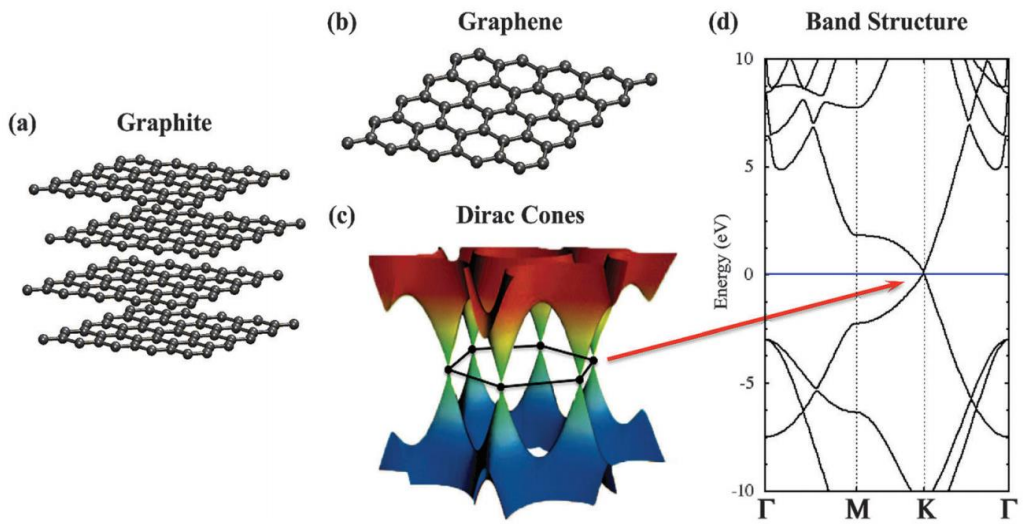


Figure 3.1 (a) Graphite structure (5x5x2 unit cells). (b) Graphene structure (5x5). (c) Dirac cones in graphene and (d) Graphene band structure (Γ-M-K- Γ). Fermi level has been shifted to 0 eV and depicted with a blue horizontal line. [104]

Graphene has a unique electronic band structure. It is a semi-metal, characterized by the absence of a band gap. The Fermi level is crossed by electronic bands near the six corners of the two-dimensional hexagonal Brillouin zone (Figure 4.1 (c) and (d)). The dispersion relation (the change of electron energy of a band within the Brillouin zone) is linear at these points, a unique feature that leads to zero effective mass for electrons and holes, and thus to very high Fermi velocities of electrons and holes. Due to this linear or conical dispersion relation, near these six points electrons and holes behave like relativistic particles described by the Dirac equation. Therefore, the electrons and holes are called Dirac fermions and the six corners of the Brillouin zone are called the Dirac points (Figure 3.1 (c)). The massless Dirac electrons at the Fermi level derive also in the highest known finite-temperature electron mobility, and it should enable transistors operating at very high frequencies beyond the standard semiconductor technology [105]. Furthermore, the extremely low spin–orbit interaction in graphene makes it an ideal spin carrier for spintronics [106]. Graphene is the world's best heat conductive material. As graphene is also strong and light, it means that it is a great material to make heat-spreading solutions, such as heat sinks [107]. Graphene is the world's thinnest material and thus it is also the material with the highest surface-area to volume ratio, so this property combined with their electrical properties makes graphene an excellent material

for storage energy applications (i.e. batteries, solar cells and supercapacitors) as it will enhance the charging speed or storage of energy [108]. The intrinsic properties mentioned above result in ultrawideband accessibility provided by the e–h pair generation in graphene, which is gate controllable, at all wavelengths. Thus, graphene can have strong light interaction and special phenomena such as light excitation of collective oscillations of carries, i.e., plasmons in grapheme, in the THz range. Furthermore, it is possible to create an inversion of the conical electronic band around the Dirac point with optical excitation [109], leading to gain in the THz range. This property makes graphene an excellent material for novel applications in the THz range [110] such as THz sensors [92], emitters [21] and modulators [111].

Nevertheless, those properties are highly influenced by the interaction of the graphene layer with the substrate. A parameter of great importance is the flatness of the substrate since a non-flat substrate will lead to a corrugation of the graphene layer, which will most likely create undesired effects. Several substrates have been used for the production and transfer of graphene sheets but Si/SiO_2 remains the most widely used one. Several methods as mechanical exfoliation and CVD use SiO_2 substrates for graphene production [112], [113]. The substrate consists of a layer of 90 or 300 nm of SiO_2 on top of a highly doped Si wafer. The thickness of the SiO_2 layer allows an easy identification of the graphene flakes using an optical microscope while the highly doped Si substrate is usually used as a back gate. The deposition of a graphene sheet on SiO_2 induces a large carrier density inhomogeneity, combined with the corrugation of the graphene sheet. This leads to a considerable degradation of the carrier mobility [114]. Similar effects can be observed on different substrates as graphene growth on copper by epitaxial growth and CVD [115] or graphene growth on SiC by Epitaxial growth [116] among other substrates [117].

4.2.2 Hexagonal Boron Nitride

Hexagonal boron nitride (h-BN) is a tridimensional crystal with the same structure that graphene and is sometimes referred to as ‘white graphene’ [118]. It consists of a stacking of atomic-two-dimensional layers (Figure 4.2 (a)). Within each layer, boron (B) and nitrogen (N) atoms are bounded by strong covalent bonds in a honeycomb-like structure, whereas the layers are weakly bound by van der Waals forces (Figure 4.2 (a)).

The different onsite energies of the B and N atoms lead to a large energy band gap of 5.97 eV (Figure 4.2 (b)), comparable to other insulators used for semiconductor technology [119]. Moreover, h-BN has a meager lattice mismatch (1.7 %) with respect to graphene. The dielectric properties of h-BN with a relative permittivity $\varepsilon \sim 3{-}4$ and a breakdown electric field $\sim$ 0.7 V/nm [120] allow the use of h-BN as an excellent gate dielectric. These properties make the h-BN the so far most suitable substrate and dielectric/separation layer for graphene electronics and optoelectronics applications

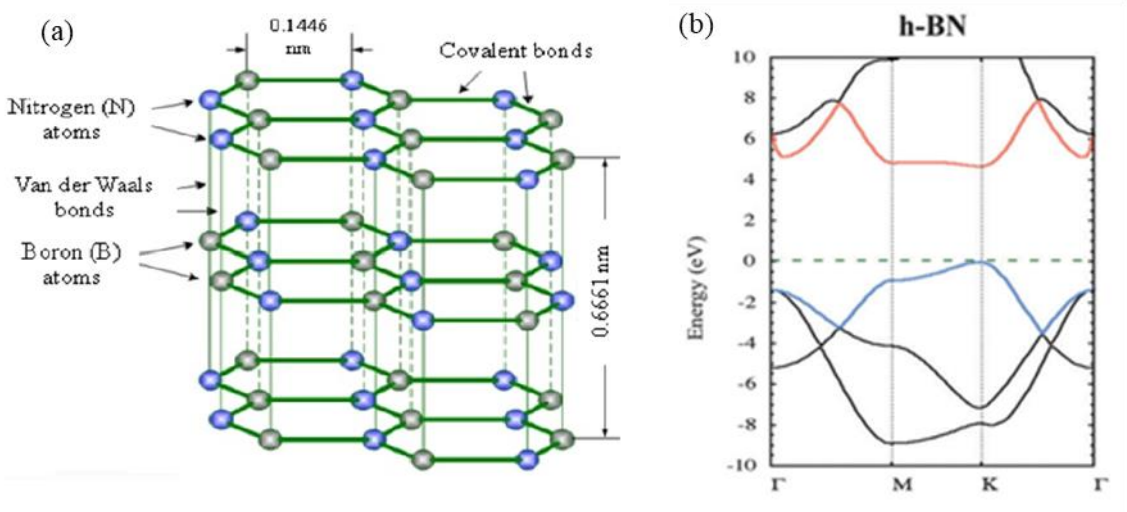


Figure 4.2 Schematic of hexagonal boron nitride (h-BN) structure (a) [121] and h-BN band diagram (b) [104]

Furthermore, h-BN flakes show high chemical stability, thermal conductivity up to 600–1000 W m^{-1} K^{-1}, an anti-oxidation temperature about 900ºC, a melting temperature around 2700 ºC, and a refractive index of 1.8. Finally, h-BN also has good process ability, such as thermal shock resistance to electrical vibration and it is non-toxic and environmentally friendly [122].

Similarly to graphene, there are several ways to produce h-BN flakes: ultrasonication [123], high-energy electron beam irradiation of BN particles [124], epitaxial growth [125] and mechanical cleavage [120]; this latter exhibits the best physical properties, quality and performance both as substrate and as dielectric.

4.2.3 Graphene heterostructures

The hardest challenges that graphene fabrication needs to overcome are: the low homogeneity & reproducibility, the small size of the flakes, and the interaction with the substrate. One emerging idea to overcome the former difficulties is to encapsulate graphene between two sheets of h-BN. Additional 2D layers may be deposited resulting in a stack of 2D materials in a given sequence (artificial 3D material)—as in building with Lego—with blocks defined with one-atomic-plane precision (Figure 4.3). Strong covalent bonds provide in-plane stability of 2D crystals, whereas relatively weak, van-der-Waals-like forces are sufficient to keep the stack together. The possibility of making graphene-based multilayer van der Waals heterostructures was demonstrated experimentally [126].

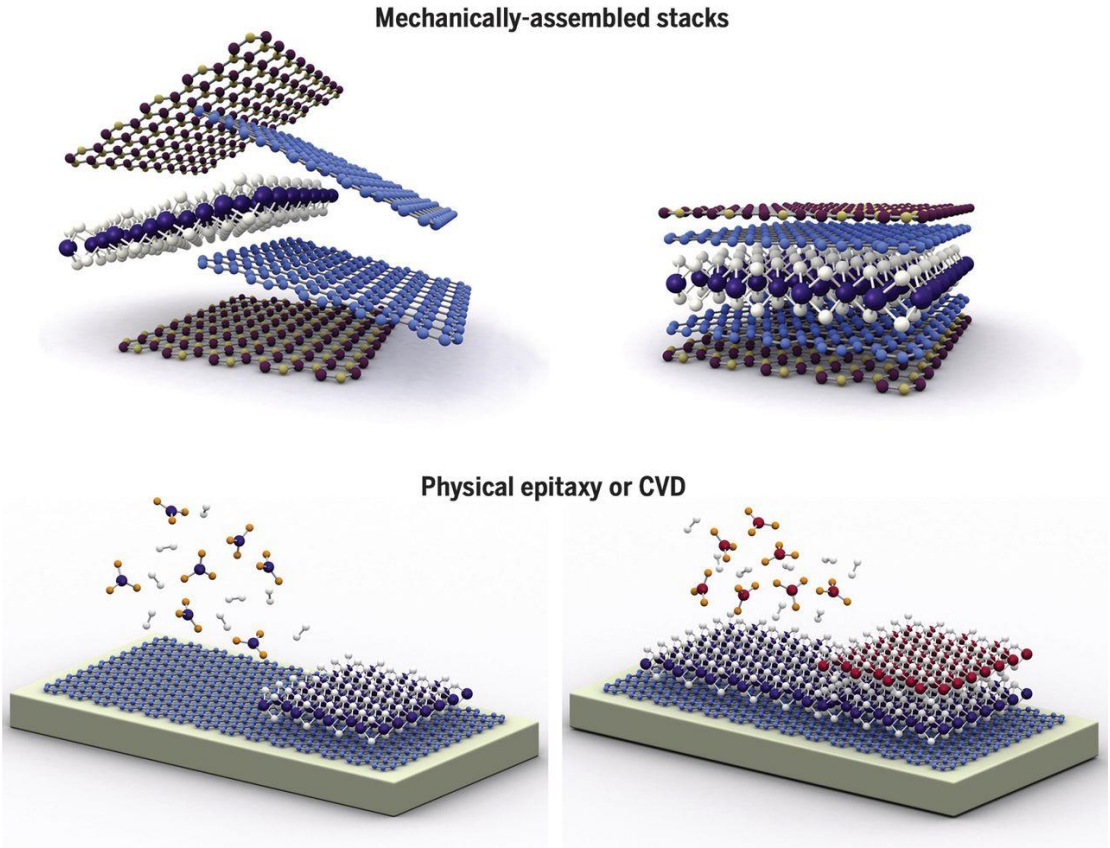


Figure 4.3 Cartoon of 2D materials and Van derWaals heterostructures. 2D materials can be combined to create new mechanical assembled stacks (top) or physical epitaxy or CVD heterostructures (bottom). [127]

The main advantage of this method relies on the fabrication of innovative and artificial devices with layered 2D materials beyond the standard graphene sheet fabricated on a commercial substrate. Those devices open a new era of devices based on 2D materials for different fields of science and for new applications.

Graphene based heterostructures obtained by growth methods such as chemical vapor deposition (CVD) or epitaxial growth are the future for scalable manufacturing of van der Waals heterostructures [128], [129]. However, a huge effort will be needed to fabricate high quality, high mobility devices for electronic and optoelectronic applications.

4.3 Asymmetric Dual Grating Gate

As stated above, asymmetry between source and drain un a FET is needed to induce photovoltaic detection (with no DC drain bias current) under THz radiation [130]. As previously discussed, there are several ways to introduce such asymmetries and few were explored using Graphene. One possibility is the difference in the source and drain boundary conditions that could be created by external (parasitic) capacitances or by

different resistances using different metals for the contacts [131]. Another way is the asymmetry in feeding the incoming radiation, by using special antennas [92] or by imposing an asymmetric design of the source and drain contact pads [132]. An additional way is to design an efficient broadband coupler of the THz radiation like a metal grating gate design [133]. Symmetric grating-gate FET detectors have been already demonstrated [134] and mostly exhibit a THz plasmonic photoresponse, which needs the application of a DC drain bias current to the device's channel. Nevertheless, Grating-gate FET structures with a symmetric unit cell design generate a weak photoresponse most probably due to some small uncontrollable asymmetry of the fabricated structures or/and caused by an asymmetric irradiation of the structures by THz beam.

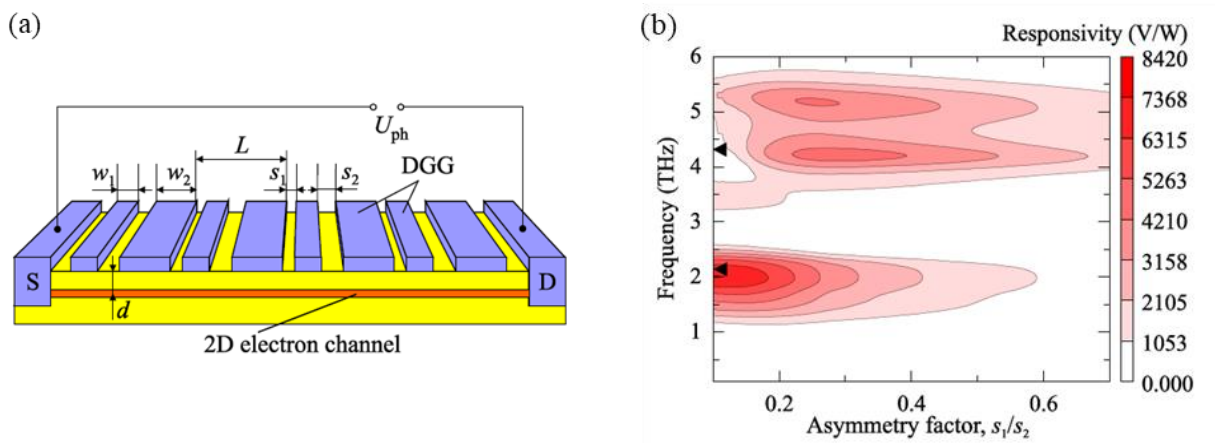


Figure 4.4 Schematic view of the double-grating-gate FET structure with an asymmetric design (a) and calculated responsivity of the ADGG-FET detector as a function of THz frequency and the asymmetry factor, s1/s2 (b).

To remedy the above problem, a novel plasmonic THz detector based on an Asymmetric Double-Grating-Gate FET (ADGG-FET) was proposed [73]. Figure 4.4 (a) shows a schematic description of the ADGG-FET. It´s formed by two interdigitated grating gates (G_1 & G_2) with widths w_1 and w_2 respectively. Fingers of gate 2 (gate 1) are separated by the ones of gate 1 (gate 2) by a distance s_1 (s_2). So that two successive slits between the DGG fingers within the ADGG-FET period are of different widths and different s_1 and s_2. This introduces the required asymmetry in the unit cell of a periodic ADGG-FET structure. Theoretical simulations performed on a device with a period L = 1300 nm, w_1 = 600 nm, w_2 = 500 nm, shows a maximum of responsivity around 8kV/W for an asymmetry factor s1/s2 around 0.1 (Figure 4.4 (b)). The asymmetry in the channel of the ADGG FET structure can be strongly enhanced by applying voltage to one of the two gates of the device. 2D plasmons are periodically localized under the fingers of one gate while the other one is depleted. Therefore, an adequate design on the ADGG structure should lead to a strong coupling under radiation of different THz frequencies and significantly enhance the photoresponse signal. ADGG-FETs fabricated on InAlAs/InGaAs/InP heterostructures demonstrated the potential of those devices as THz detectors exhibiting strong photovoltaic responses under THz radiation at room temperature [135], [136].

4.4 Devices fabrication

In this section, we will describe the process of the fabrication of Asymmetric Dual-Grating-Gate Graphene FETs used in this Thesis for terahertz detection. The structures fabrication starts by the production of graphene (mono or bilayer) and h-BN by mechanical exfoliation. The graphene layer was sandwiched between two layers of h-BN and then processed to fabricate ADGG-GFETs.

4.4.1 Graphene and h-BN production and characterization

The first process in the fabrication of graphene FETs is, therefore, the production of high-quality graphene layers (mono or bilayer) on a Si/SiO_2 substrate by mechanical exfoliation. This method traditionally provides the best quality graphene sheets with the best electrical properties. It´s also known as the Scotch^{TM} tape method [137], and was firstly developed by Geim and Novoselov in 2004 [20], [138]. The first step of the process is the cleaning of the Si/SiO_2 wafer with acetone to remove any impurity and get a clean surface. Then, the sample is placed into an ultrasonic bath for two minutes. To remove residues of acetone, the wafer is submerged in ethanol (or 2-propanol) for 30 seconds. Finally, to remove any water or remaining alcohol, the wafer is heated to temperatures above 110 ^{o}C.

Few thick flakes of natural graphite are placed on an adhesive tape (Scotch tape) and folded onto itself. The graphite flakes are peeled off when the Scotch tape is unfolded, so the area of the tape with graphite flakes is increased. This peeling process is repeated several times, which gives rise to a relatively large area of progressively thinner graphite flakes spreading on the tape. Then the graphite flakes are “exfoliated” on SiO_2 (previously prepared) by applying a small pressure on the tape when it is placed on the substrate. Finally, the tape is removed slowly and then a few flakes of different thickness will be released on the substrate (Figure 4.5 (a)). The thickness of the SiO_2 is around 300nm allowing the highest optical contrast with the graphene under the optical microscope. The contrast between the graphene flake and the 300nm thick SiO_2 is at its maximum (12%) under incident light of 550 nm [139], [140]. Furthermore, thick graphite flakes have a yellowish color, fading into blue colors as the thickness decreases and turning finally into light purple for few layers graphene. Figure 4.5 (a) shows graphene flakes obtained on SiO_2/Si wafer.

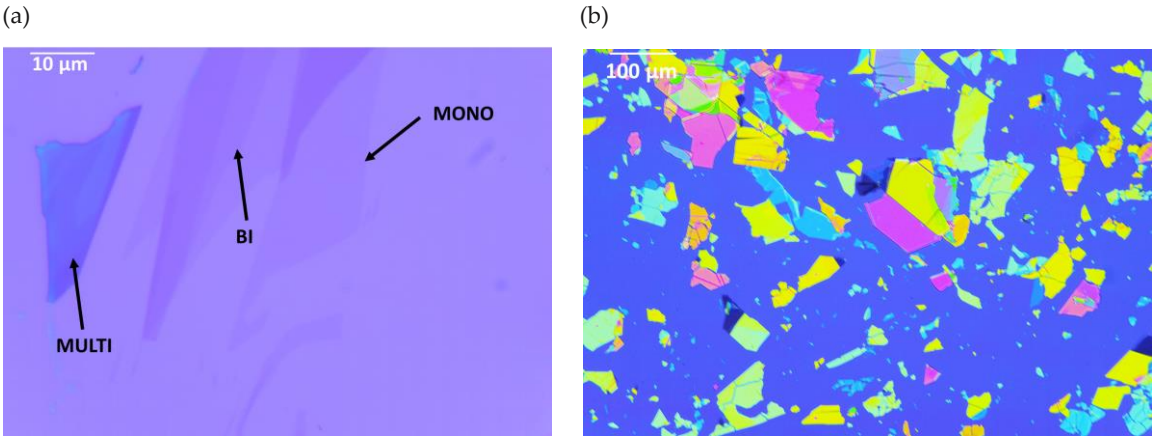
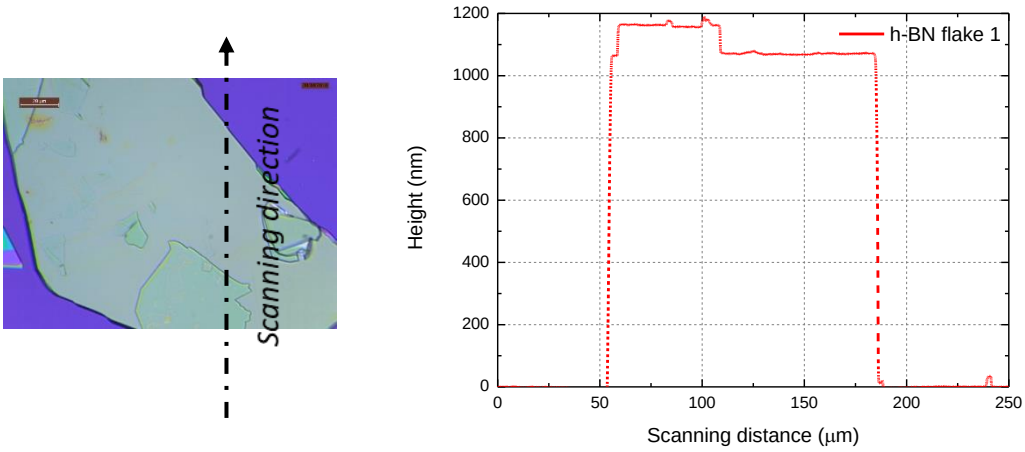


Figure 4.5 (a) Optical images of graphene (monolayer, bilayer and multilayer) and (b) h-BN flakes

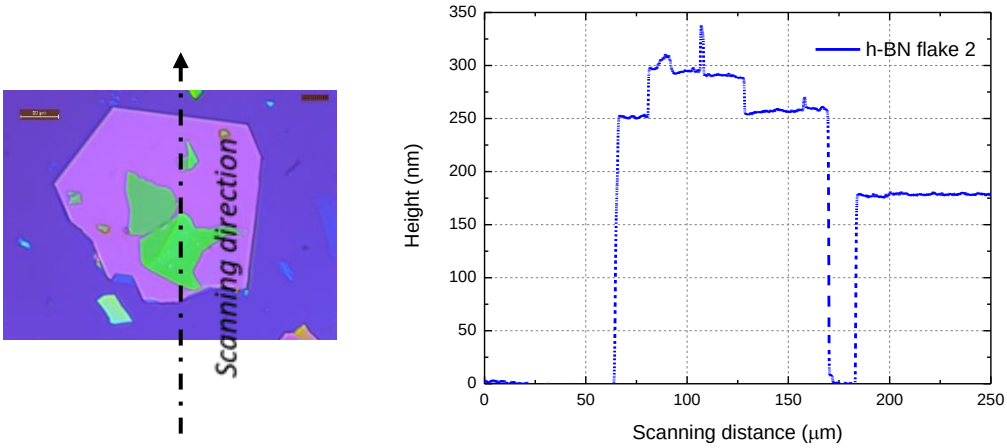
Mechanical exfoliation provides fakes relatively small of moderate area (~10x10 μm^2). Additional steps were introduced to increase the area of the graphene flakes [141]: Prior to the exfoliation process, ambient adsorbents were removed from the substrate using an oxygen plasma cleaner. Moreover, additional heating when the tape has been stuck onto the substrate can maximize the area of those crystals. Those steps give an increase of the area of the obtained flake by a factor of five. The graphene flakes are located by optical microscopy and then characterized by microRaman spectroscopy.

The next step is dedicated to the exfoliation of h-BN. Ultra-pure bulk h-BN crystals used for the exfoliation was obtained from our collaborations with Research Institute of Electrical Communication at Tohoku University (Sendai, Japan) and National Institute of Material Science (Tokyo, Japan). The same process was used for the exfoliation (Figure 4.5 (b)) of h-BN. As we mentioned, h-BN is a large band-gap insulator, which can be employed as dielectric material to electrically isolate the graphene from metallic contacts and environment. Relatively thick h-BN flakes must be obtained to ensure that the graphene is isolated from the gate's contacts to avoid leakage current throught the insulator as the breakdown electric field is approximately 0.7 V/nm. To this aim, h-BN flakes were characterized using a DektakXT stylus profiler (Figure 2.9). This profiler provides a nanometric resolution and may generate a 3D topographical mapping. As the h-BN flakes must be relatively thick (>10 nm) [142] the stylus profiler is sufficiently precise to measure their thickness. More information about the DektakXT stylus profiler can be found on Section 2.5.1. The results showed in Figure 4.6 are in excellent agreement with the above discussion about the optical contrast.

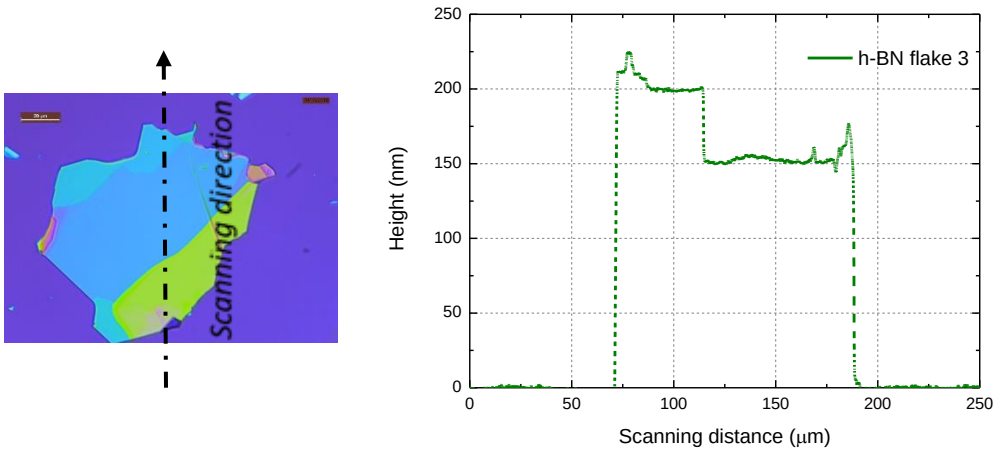
(a)


Scanning direction
h-BN flake 1
Height (nm)
Scanning distance (μm)
0
200
400
600
800
1000
1200
0
50
100
150
200
250

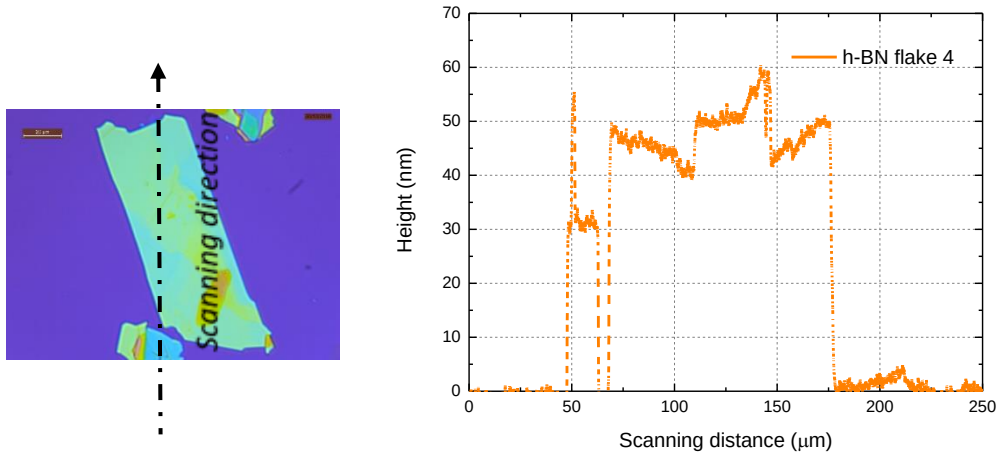
(b)


Scanning direction
h-BN flake 2
Height (nm)
Scanning distance (μm)
0
50
100
150
200
250
300
350
0
50
100
150
200
250

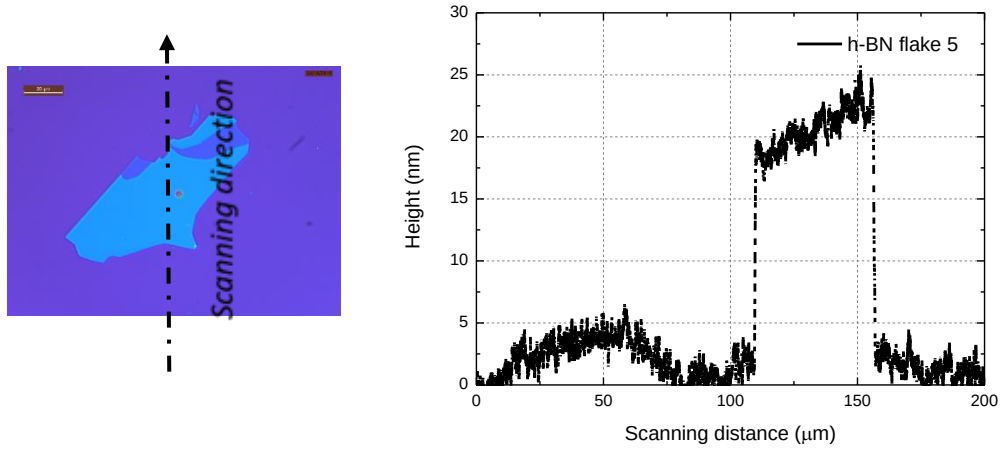
(c)


Scanning direction
h-BN flake 3
Height (nm)
Scanning distance (μm)
0
50
100
150
200
250
0
50
100
150
200
250

(d)



(e)



(f)

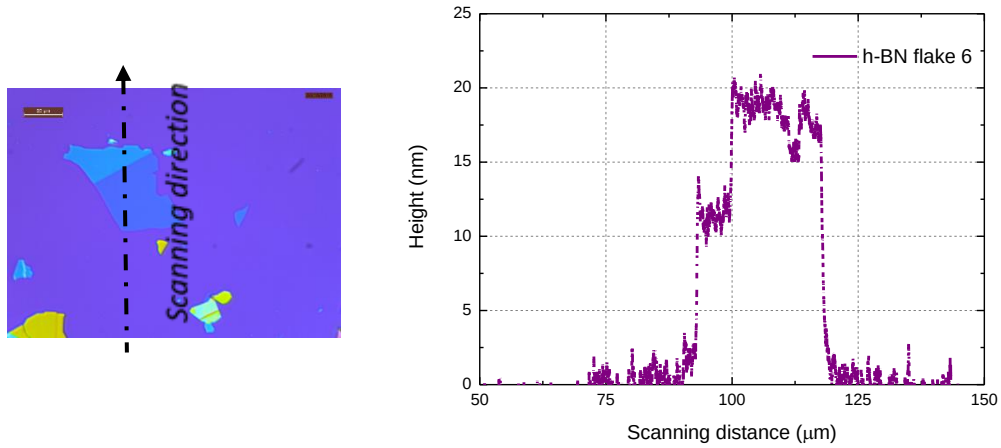


Figure 4.6 Optical images (left) and their profilometer measurements (right) of different h-BN flakes (a)-(f).

Figure 4.6 shows both the optical image (left) and the profile measurements (right) of different h-BN flakes with different thickness. The dashed arrow shows the scanning direction of the h-BN flake for each plot. A relatively thick h-BN flake (~µm) shows a greenish color, fading then progressively change into purple, yellow with decreasing thickness and goes to blue for 250-150 nm thickness range. For the sub-50 nm range, it is quasi-transparent turning to blueish color for a few layers h-BN (<10 nm). The available equipment has a vertical nanometric resolution that is not adequate to characterize graphene (also few graphene layers) or thin h-BN flakes. Moreover, as this is a contact technique, the material can be easily damaged while measuring. To characterize those materials, especially single and few graphene layers, microRaman spectroscopy is the choice. It is a very strong, fast and contactless technique [143]. Moreover, Raman spectrum provides information related to the quality of the material, i.e. graphene and h-BN, before processing. A visible laser at 532 nm with an output power of 100 mW (attenuated down to 1 mW) was used to excite the sample. A diffraction grating of 600 mm/gr was used to provide a frequency shift resolution of 2 cm^{-1}. More information related to the MicroRaman spectrometer used in this Thesis work is provided on Section 2.5.2.

The main features of the Raman spectrum of graphene and graphite (carbon materials in general) are the so-called D and G bands, which lie around 1360 and 1560 cm^{-1}, respectively. D band is only observable in graphene/graphite with defects as an additional peak called D' [144]. An additional intense peak emerges near 2700 cm^{-1}, historically known as G'. Since it is the second most intense peak observed in graphite samples [145], and because is the second order of the D, it is called 2D [146]. Around 3250 cm^{-1}, an additional peak is observed and called 2D' as it is the second order of the D' peak [147].

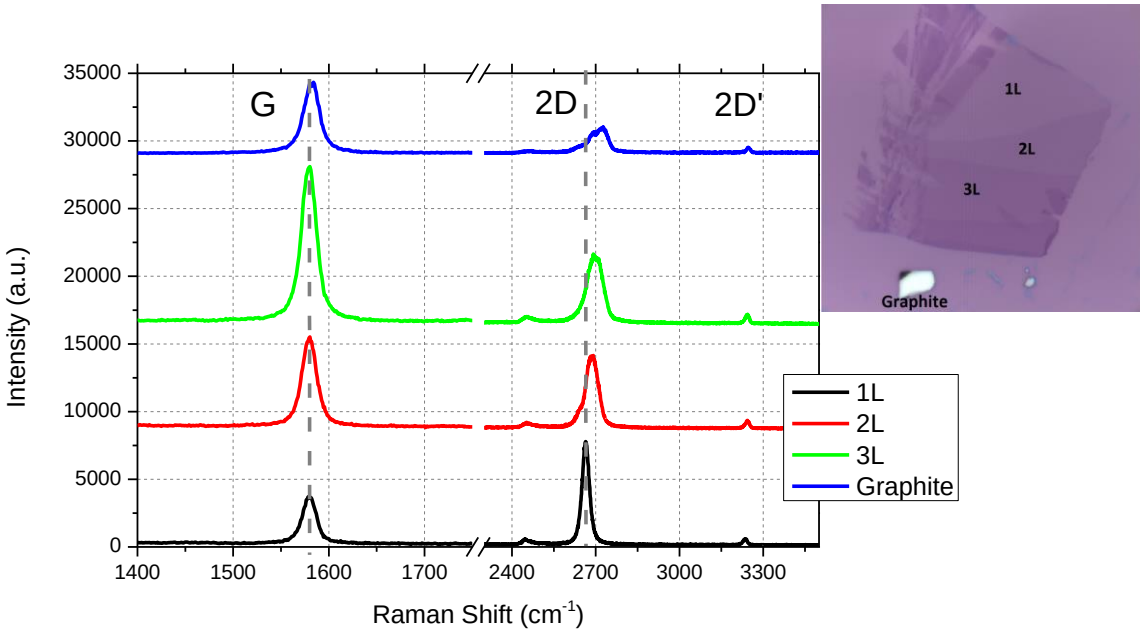


Figure 4.7 Optical image of different Graphene flakes (mono-, bi-, tri- and multi- layer) and their Raman spectrum.

Figure 4.7 shows the optical image of mono- (1L), bi- (2L), tri- (3L) and multi- (Graphite) layer graphene samples (a) and their respective Raman spectrums (b). The 2D peak shows a considerable change in its intensity, shape and position when the number of layer decreases. Monolayer graphene shows an intense and sharp 2D peak, approximately 2 times more intense than G peak. It is symmetric and can be fitted using a Lorentzian function. The intensity of the 2D peak (I2D) decreases, becomes broader and it is upshifted to higher energies when increasing the number of layers up to graphite. However, the intensity of the G peak (IG) increases when increasing the layers and the I2D/IG ratio becomes lower. No D peak was observed on the exfoliated graphene samples (Figure 4.7), demonstrating the high quality of the obtained graphene flakes since this peak is related to defects in graphene. The I2D/IG peaks ratio factor is an essential parameter that indicates the quality of monolayer graphene samples [148]. This factor is around 2 for exfoliated graphene on Si/SiO_2 and increases to 3 if the substrate is treated with HDMS [149] compromising the area of the exfoliated flakes. The adhesion of graphene to Si/SiO_2 substrates is increased if the substrate is previously treated with O_2 plasma but the factor is reduced below 2 [150]. Graphene (Gr) based heterostructures (h-BN/Gr/h-BN) emerge as a good candidate that offers both features: (i) relatively large and homogeneous flakes could be obtained and (ii) a factor of I2D/IG beyond 4 on fully encapsulated samples can be reached [151]. Analysis of the Full Width at Half Maximum (FWHM) of the 2D band peak is also used to characterize the flakes. Monolayer graphene shows a FWHM close to 26 cm^{-1} while bilayer graphene exhibits a value of 52 cm^{-1} [152]. For three and four-layers graphene, the FWHM was around 56.1 cm^{-1} and 62.4 cm^{-1}, respectively. For few graphene layers thicker than five layers, the Raman spectrum and then the FWHM is hardly distinguishable from bulk graphite. Our experimental results showed that mono-, bi- and tri- layer graphene exfoliated on SiO2/Si exhibit a 2D FWHM around 30.5 cm^{-1}, 51.9 cm^{-1} and 61,9 cm^{-1} in agreement with other studies [152].

Figure 4.8 shows the Raman spectra of the same h-BN flakes previously characterized by the profilometer (Figure 4.6) where a single peak was observed around 1365 cm^{-1}. This peak is attributed to the first order Raman effect related to the B-N vibrational mode within h-BN layers [153], [154]. No second order or additional peaks were observed beyond the frequency shift range showed on Figure 4.8. We found that the peak intensity obtained from the Raman measurements for the h-BN flakes is directly proportional to number of layers. Thus, the Raman measurements for a given substrate were calibrated (i.e. Si/SiO_2 in our experiments) with the profilometer measurements and optical contrast, allowing us to estimate the thickness of the h-BN layer without performing any direct contact technique measurements. For higher accuracy, AFM profile measurements followed by Raman spectrometer are used to identify the number of h-BN layers [155].

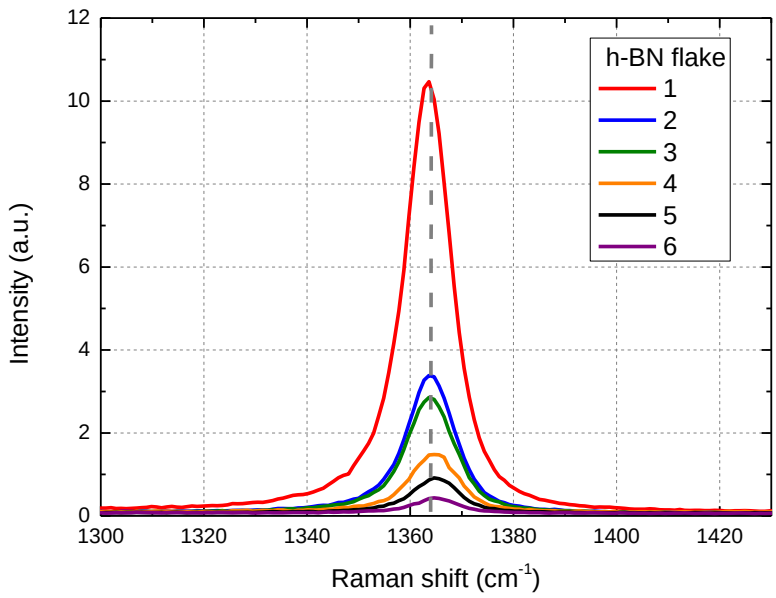


Figure 4.8 Raman spectrum of h-BN flakes showed on Figure 3.6

4.4.2 Graphene heterostructures

A new in-house developed setup (Figure 4.10) was installed in our clean room to encapsulate graphene between two flakes of h-BN. This procedure allows to enhance the quality of the graphene layer (for instance, to obtain high carrier mobility). First, a monolayer (or bilayer) graphene (Figure 4.9 (b)) and two h-BN flakes top (Figure 4.9 (a)) and bottom (Figure 3.9 (c)) for encapsulate the graphene must be fabricated using the mechanical exfoliation method exposed before. All the flakes were characterized by both optical contrast and Raman spectroscopy to ensure the quality of the flakes.

(a) (b) (c)

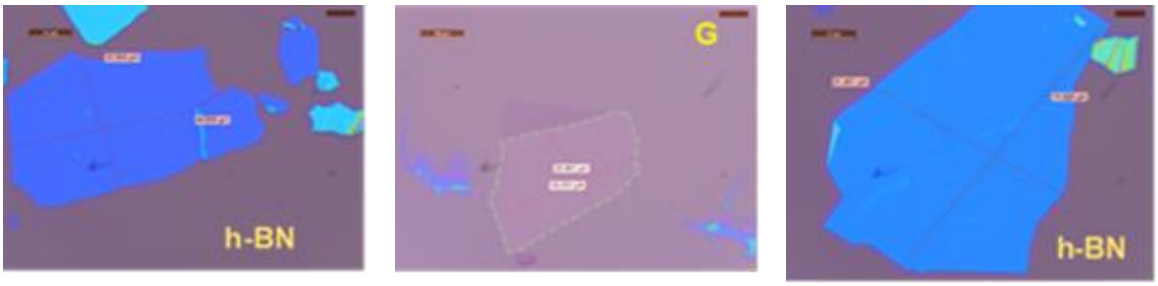


Figure 4.9 Optical images of h-BN (a) and (c) and graphene (b).

There are several methods to transfer 2D materials onto another substrate [126]:

- PMMA carrying layer method [120]
- Sacrificial layer-based transfer method [156]
- Wedging transfer method [157]
- PDMS deterministic transfer method [158]
- Van der Waals pick-up transfer methods [159]

The former one is a dry transfer method based on a polymer stamp used to pick up the graphene sheet and h-BN flakes toward the assembly of graphene heterostructure. This method was introduced by Wang et al. [160] and ensured high quality graphene samples since the graphene sample wasn´t in contact with any polymer throughout the whole process, reducing the impurities being trapped between the layers. Since then, some modifications to the transfer method were introduced to improve the layer quality by modifiying the polymer stamp or the steps on the transfer route [159], [161]. A variation of the work described in [162] is employed in this work to fabricate graphene heterostructures.

The stamp employed on the transfer method is based on a polypropylene carbonate (PPC) solution coated by a polydimethylsiloxane (PDMS) film working as a carrier layer and then placed on a glass slide. The whole set is crucial to pick and drop the 2D materials.

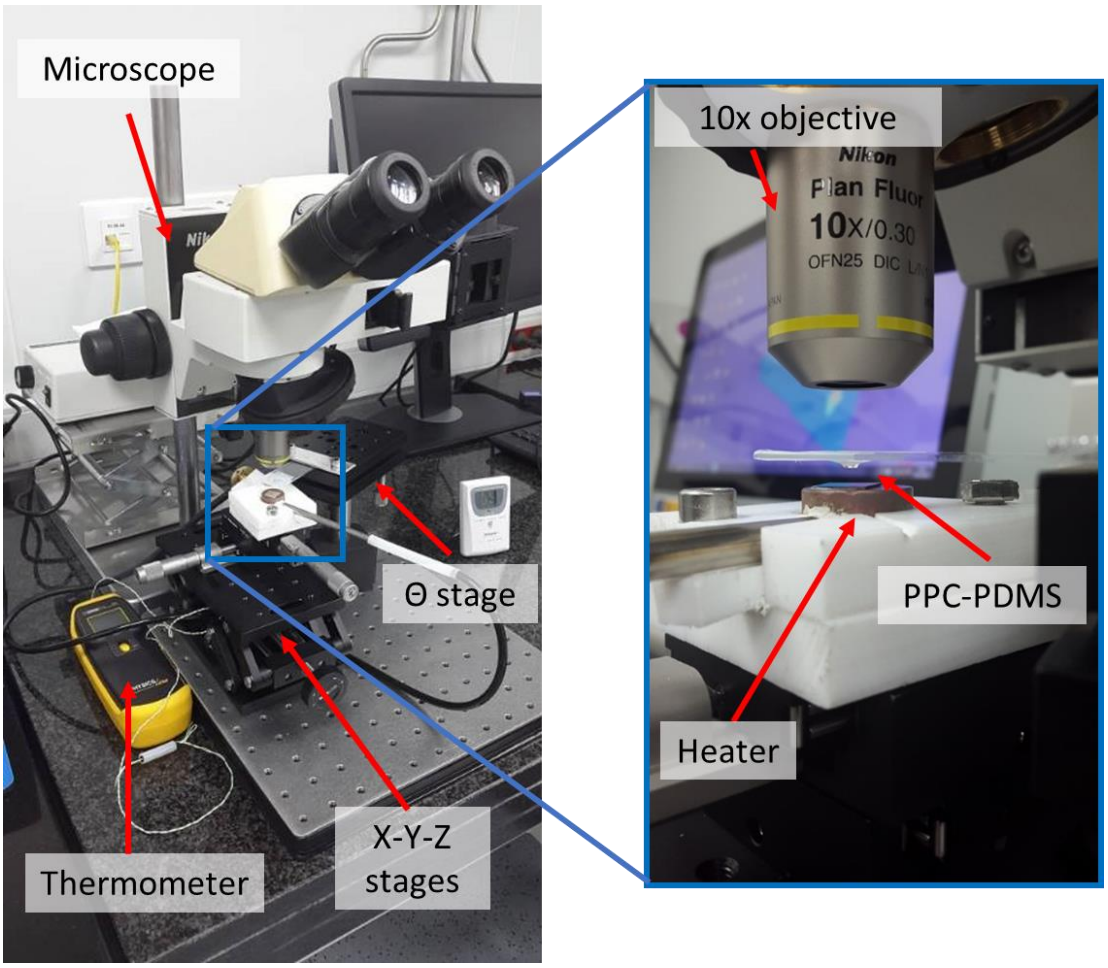


Figure 4.10 Experimental homemade setup employed for the dry transfer process (left) and zoomed image (right)

The transfer system is shown in Figure 4.10 where all the process is done under an optical microscope (Nikon microscope) with a large focal distance optical objective (Magnification x10, Numerical Aperture 0.30, Working Distance 16 mm) to identify the flakes (graphene & h-BN). An XYZ micrometer stages with a heating plate is used to accurately place the substrate under the stamp. The stamp, attached to a tilting micromanipulator, ensures a high degree of freedom in the alignment of the 2D crystal flakes. As the stamp is transparent, it is possible to see the substrate through it and thus perform the alignment. The substrate is fixed with vacuum and heated during the transfer process.

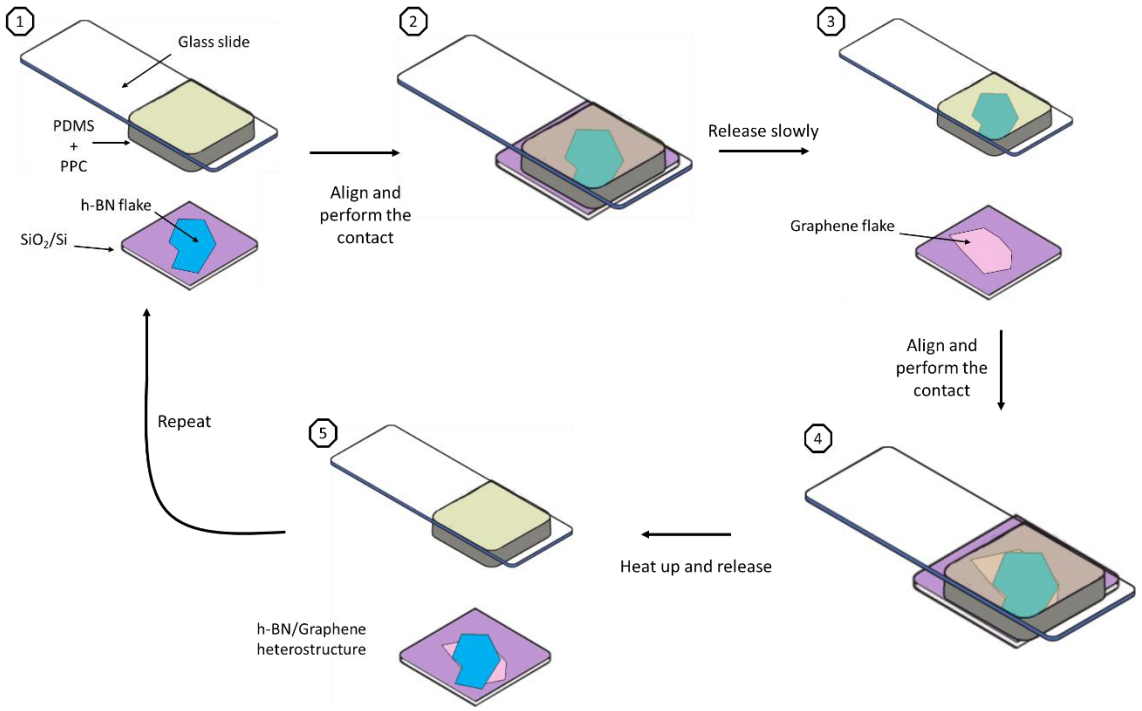


Figure 4.11 Schematic image of the dry transfer technique for the assembly of van der Waals heterostructures

Figure 4.11 shows a schematic view of the transfer process employed in the fabrication of the graphene heterostructures at the USAL clean room. This process is described as follows:

1. The top h-BN flake is located on the Si/SiO_2 substrate. The stamp is placed over the Si/SiO_2 substrate with the top h-BN and, then, by using the micrometer stages and the optical microscope, the top h-BN flake (Figure 4.9 (a)) is located and positioned under the stamp. As the stamp is quite transparent, the h-BN flake can be located throught the stamp on the Si/SiO_2 substrate.

2. The sample is aligned with the stamp by using the XY micromanipulator and then raised to perform the contact with the stamp. After, the temperature of the substrate in increased up to 40 ^{o}C and, using the Z micromanipulator, the PPC will cover the whole flake.

3. The top h-BN flake is picked up by the stamp. Increasing the temperature up to 40°C allows to pick up the top h-BN flake with the stamp. Then by using the Z micromanipulator, the Si/SiO2 substrate is slowly lowered until the stamp and the substrate are separated and, then, the top h-BN will be picked up from the substrate by the stamp. As the stamp is transparent, the optical contrast of the h-BN flake picked up by the stamp is very different, but it can be located on it. (Figure 4.12 (a)). Then the graphene flake (Figure 4.9 (b)) on Si/SiO_2 is placed on the sample holder, and then the alignment is performed through the transparent stamp, along with the top h-BN, with the micromanipulators.

4. The h-BN flake can be transferred somewhere else; i.e the graphene flake, which is aligned with the top h-BN flake picked-up on the stamp by following the step 2. The graphene flake or the h-BN flake (i.e. the stamp) can be rotated before performing the contact to ensure a proper alignement of both flakes.

5. The top h-BN flake is deposited on the graphene. The temperature of the substrate with the graphene is increased up to 100 ^{o}C enabling a reduction of the adhesion between the PPC and the h-BN flake and, accordingly, to enhance the Van der Walls force between the h-BN and graphene flakes. Therefore, the h-BN flake is deposited on the graphene flake reaching the above temperature. The result is a h-BN/Graphene heterostructure on the Si/SiO_2 substrate (Figure 4.12 (b)). Some residues from the PPC film can be deposited around the heterostructure as consequence of the high temperature. (Figure 4.12 (b)). Nevertheless, the graphene is covered by the h-BN and then is not exposed to these residues. Moreover, the heterostructure as well as the substrate can be cleaned easily following the steps described on section 4.4.1.

6. The last step is to pick up the obtained stack (h-BN/Graphene) with a new stamp and then putting it on the bottom h-BN flake (Figure 4.9 (c)). The same process, as presented on steps 1-5, is repeated subsequently (Figure 4.11). Upon completion of all the above steps, the entire vertical h-BN/Graphene/h-BN heterostructure is obtained (Figure 4.12 (c)).

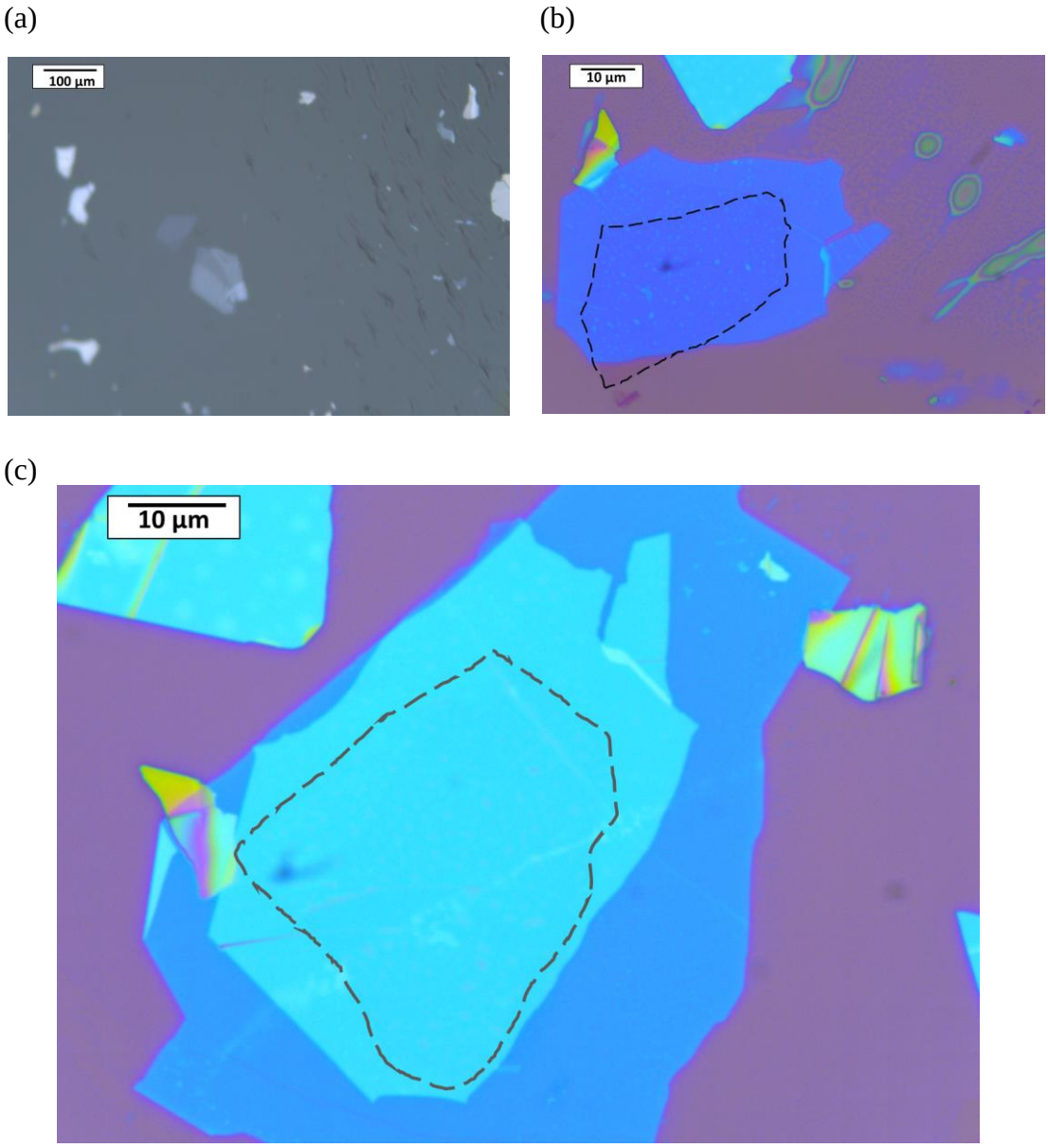


Figure 4.12 Optical images of some flakes detached by the PPC film (a) and a h-BN/Graphene heterostructure (b). Complete h-BN/Graphene/h-BN heterostructure placed on a Si/SiO_2 substrate

Finally, the sample is immersed in anisole solution to dissolve the PC residues deposited on the surface after the completion of the transfer process. Then, the heterostructure is cleaned following the procedure detailed in section 4.4.1.

The described process enables the fabrication of h-BN/graphene/h-BN heterostructures where the graphene is completely encapsulated by the h-BN layers ensuring high quality and non-exposition to polymers. A key feature of the developed technique is its ability to produce high-quality graphene heterostructures. Moreover, the capability of working with a tilting micromanipulator allow the fabrication of high-quality blisters-free graphene heterostructures, as we can tune the speed during the assembling of the different 2D flakes. This technique, valid for a high number of 2D

crystals, opens a new way to the production of high quality and non-natural heterostructures and the combination of different crystals

The obtained heterostructures were characterized by Raman spectroscopy to test and ensure a high-quality of the graphene sheet. Figure 4.13 shows the Raman spectrum of the final h-BN/Graphene/h-BN heterostructure on a SiO_2/Si substrate. It can be observed that the obtained ratio is higher than 7 (Figure 4.13), this indicates a high-quality of the fabricated graphene van-der-Walls heterostructures. This high-quality of the layers leads to high carrier mobility and clean interfaces. Those results are also supported by electrical measurements. Moreover, a significant alteration on the 2D band FWHM was found. The h-BN/G/h-BN heterostructure on a SiO_2/Si substrate exhibited a FWHM value close to 18.6 cm^{-1}, while in the graphene flakes were above 30 cm^{-1} on SiO_2/Si. This can be explained by structural deformations that broaden the 2D band and increases the FWHM value [151].

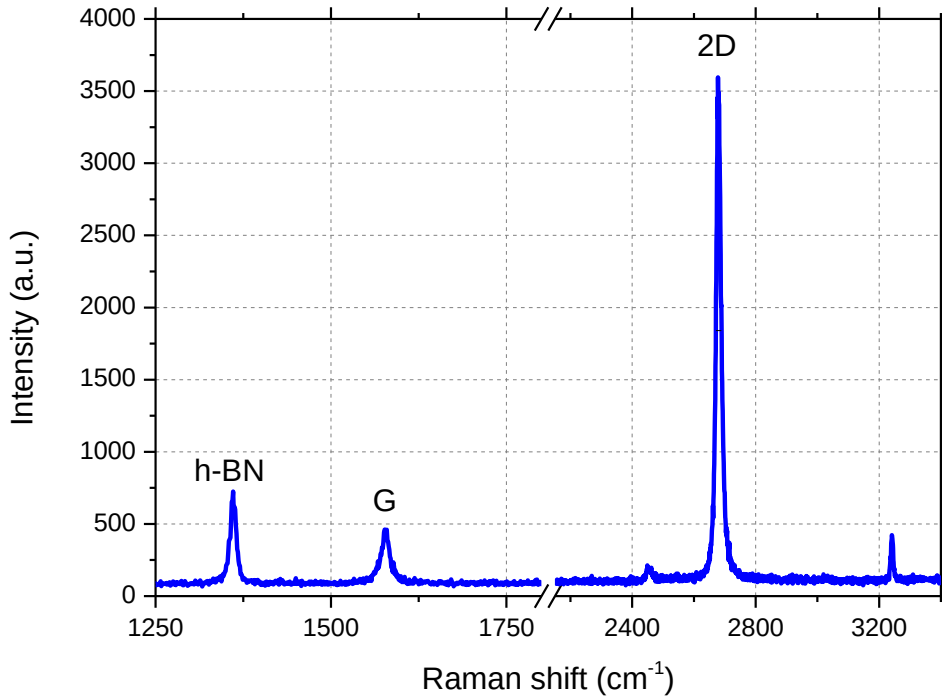
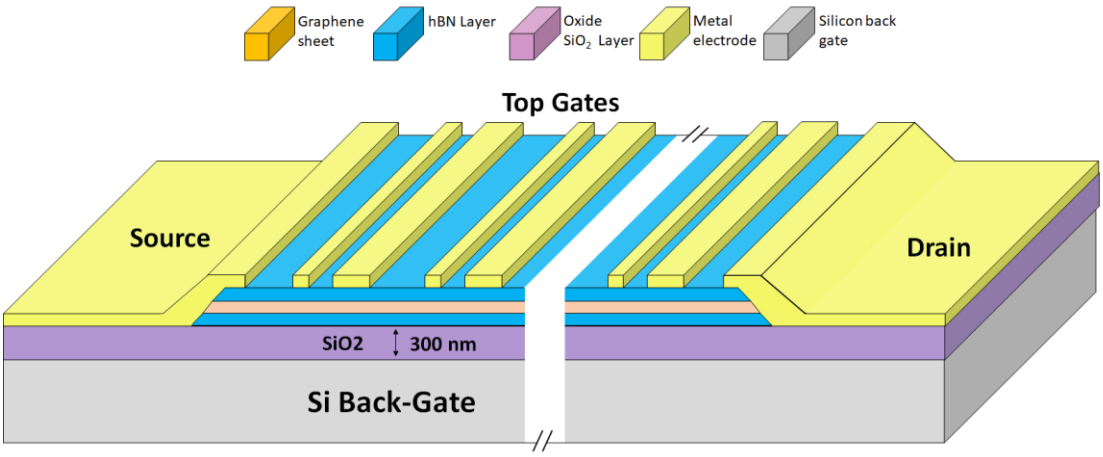


Figure 4.13 Raman spectrum of the fabricated h-BN/Graphene/h-BN. Intensity peak ratio (I2D/IG) is around 8.

4.4.3 ADGG-GFETs fabrication process

It has been both theoretically and experimentally demonstrated that the use of a multi-finger dual-gate topology greatly improves considerably the performance of THz detectors based on plasma-waves [136] (section 4.3). To this aim, an asymmetrical dual grating gate FET based on graphene heterostructure was fabricated. Figure 4.14 shows the schematic description of side (a) and top (b) views of an ADGG-GFET.

(a)



(b)

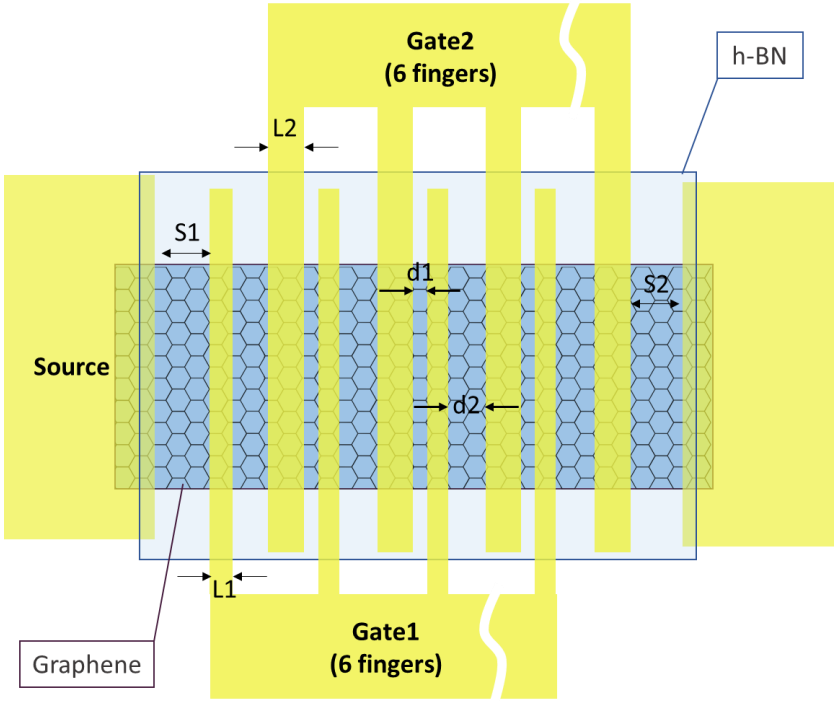


Figure 4.14 Schematic lateral (a) and top (b) views of the AGDD-GFET

Figure 4.15 summarizes the fabrication process of the transistor from the graphene heterostructure till the final ADGG-GFET. The complete process can be divided in three different sections: Bar definition, fabrication of the external contacts and fabrication of the top gates.

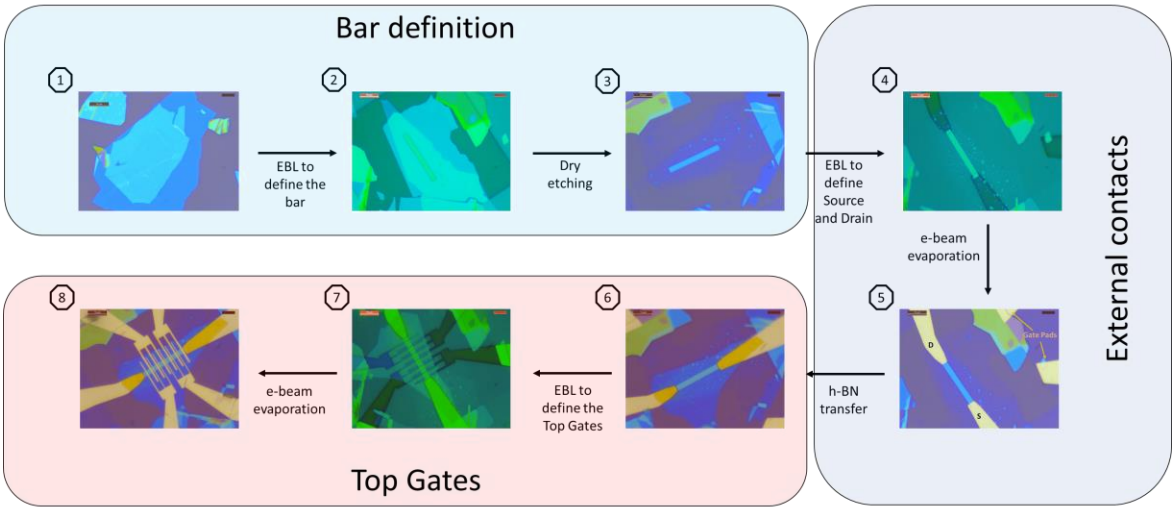


Figure 4.15 Schematic image of the fabrication process of the ADGG-GFETs. The fabrication process can be divided in three subprocesses: Bar definition, external contacts and top gates processes.

The procedure for the fabrication of these devices can de described as follows:

4.4.3.1 Bar definition

1. Firstly, the device geometry was adapted to the geometry of the fabricated heterostructure (Figure 4.15 (1)). Graphene heterostructure is located with the alignment gold marks on the SiO_2/Si substrate with a period of 400 µm (Alignment mark 1, Figure 4.16). Those alignment marks are used as spatial references. The geometry of the heterostructure, as well as the marks period, can be measured with the optical microscope using a commercial calibrated software (LAS software). The CAD design was made using the commercial software for nanolithography ELPHY^{TM}. Nanoelectronic lithography was used to pattern the CAD design on our sample. Figure 4.16 shows the CAD design of the device: (a), outer view of the design with the contact pads, and, (b), zoom view of the inner design with the dual grating gates (G1 & G2, pink color), Source (S) and Drain (D) contacts in goldish color. The dimension of the external pads was 100x100 µm^2 for Au wire bonding. Alignment marks on SiO_2/Si substrate were used as reference points (reddish squares – alignment mark 1) points in nanolithography. An additional one was designed with higher accuracy (alignment mark 2 – blueish squares) for the fabrication of the Top Gates.

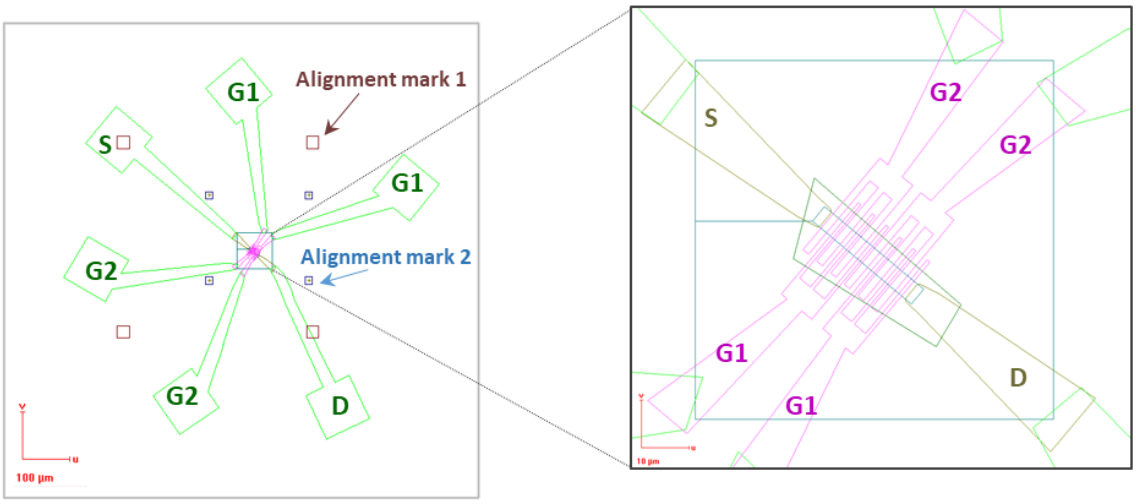


Figure 3.16 ADGG-GFET desing for the lithography processes (left) where the pads can be identified. A zommed image (right) shows the square mask for the bar definition as well as the drain and source contacts and the asymmetric gates.

2. A few milliliters thick photoresist PMMA (Poly Methyl MethacrylAte - ARP 679.04) was deposited on the heterostructure sample by spin coating. The spinner was set to a rotation speed of 4000 rpm (with an acceleration of 1000 rpm/s^2) for 60 second. This allows a coating by a homogeneous and thin (~230 nm) film of PMMA. Then, the sample was baked for 10 minutes at 160 ºC. After, the first pattern (4x30 µm bar, Figure 4.17 (a)) was performed with the electron beam lithography (EBL). EBL of the Mask was performed by using a Field Emission Scanning Electron Microscopes (FE-SEM) SIGMA with a Nanolithography Controller with a dose of ~ 270 µC/cm2 at 15 keV beam). After the lithography step, a developer (AR600.56) was used to remove the exposed areas for 2 min and then it was submerged in 2-propanol for 30 s to stop the development process.

(a) (b)

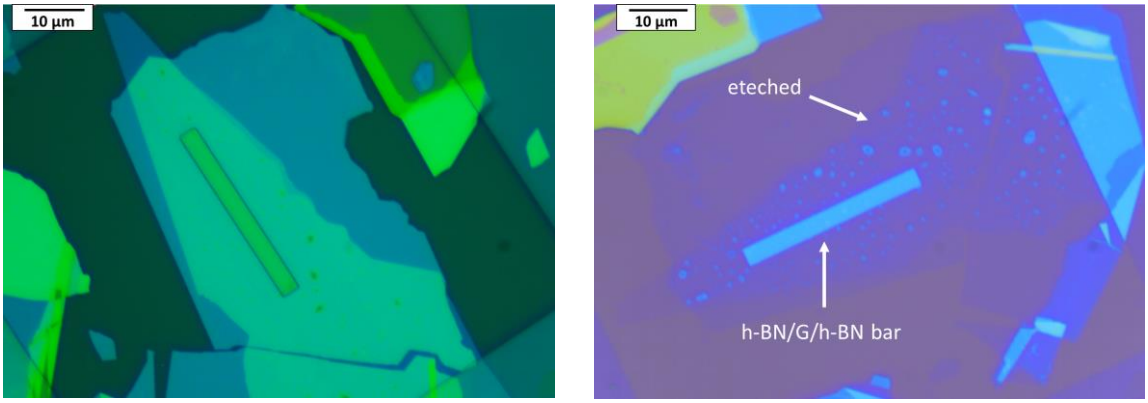


Figure 4.17 Graphene heterostructure after the mask has been patterned by e-beam lithography (a). The bar is still covered by PMMA working as a mask on the dry etching process. Optical image of the graphene heterostructure bar after been etched (b).

3. To complete the design of the bar, the sample was etched to define the desired geometry. The etching was performed using plasma Reactive Ion Etching (RIE) with SF_6 as a precursor. The PMMA photoresist was used, in this phase, to protect the geometry of interest of the graphene layer. The uncovered areas (SiO_2, hexagonal boron nitride) were etched away. The power was fixed to 40 W and the etching time was adjusted to the thickness of the heterostructure. For longer etching time, the plasma reacts with the resist and may lead to over-etching. We found that SF_6 plasma has a selectivity of 3:1 when etching the h-BN/graphene heterostructures with respect to PMMA. The recipe was adjusted to get a pyramidal profile on the graphene heterostructure bar to obtain a high-quality quasi one-dimensional ohmic contacts. The sample is then cleaned to remove the remaining resist (section 4.4.1) and inspect at the by microscope to ensure a correct definition and that sample is free of breaks (Figure 4.17 (b)). An additional step was introduced to remove residues of PMMA and bubbles on the heterostructure. This step consists of an annealing of the sample at 350º C (evaporation temperature of PMMA) and for 9 minutes while flushing with Argon in a RTA AS-ONE 100 furnace. More information about the RTA AS-ONE 100 can be found on section 2.4.3. It has been observed that below 500ºC the annealing can help to reduce the number of bubbles encapsulated in the graphene heterostructure [126]. After this step, the surface of heterostructure presents larger clean areas as compared to the initial one leading to better properties of the heterostructure such as an increased carrier mobility.

4.4.3.2 Processing of the external contacts

4. The objective on this step is to pattern the drain and source edge contacts on the graphene heterostructure bar as well as the corresponding pads for the final Au wire bonding. We used a second e-beam lithography to pattern the external pads of the gates and the secondary alignment marks spaced by 100 µm (alignment mark 2 - Figure 4.16). The sample wass spin-coated again with PMMA and baked (subsection 4.4.2) to perform a second EBL. Doses of 250 µC/cm^2 for the contacts and ~ 400 µC/cm^2 for the pads were used. Finally, the sample was developed (Figure 4.18).

(a) (b)

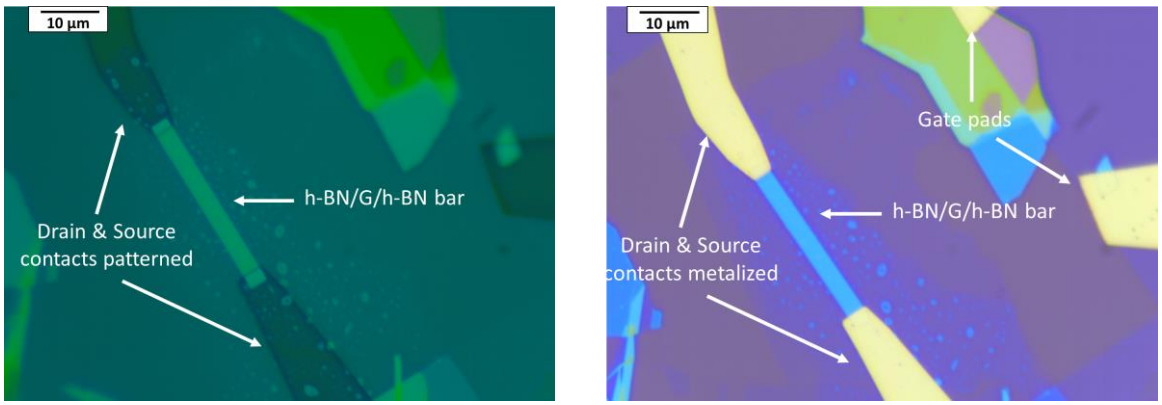


Figure 4.18 Optical image of the graphene heterostructure after the drain and source contacts has been patterned by e-beam lithography (a). The graphene heterostructure after the source and drain contacts and the gate pads were metalized (b).

5. After the sample was loaded into the e-beam evaporator chamber. This system has a long distance between the target and the sample and works at very low pressures (<10^{-9} mbar) ensuring a high control on the evaporation rate to create high homogeneity thin films More information about the e-beam evaporator can be found on section 2.4.4. Electron beam evaporation of Chromium (Cr) with 5 nm and gold (Au) with 40 nm at low rate (< 2Å/s) was selected to ensure high-quality of the edge contacts and relatively low resistance [160]. The e-beam evaporation was performed using an emission current of ~35 mA and ~270 mA and an evaporation rate of 1.5 Å/s and 1.3 Å/s for Cr and Au, respectively. After the evaporation step, a standard lift-off process removed the undesired Cr/Au metal on the photoresist. The sample was then immersed in warm acetone at 40-60 ºC (to dissolve and remove the resist and the chromium and gold still attached to it) during several minutes, until the film of gold starts to separate from the sample. A smooth flow of acetone can be then applied with a syringe to help the process. However, strong flows of acetone or ultrasonic baths should be avoided, since it usually breaks the contacts on the sample. Then, the sample was cleaned as described in section 4.4.1. Figure 4.18 (b) shows the obtained result of the graphene heterostructure bar with drain and source metallic contacts.

4.4.3.3 Processing of the top gates

6. To process the top gates of the ADGG-GFET, a new relatively thick h-BN flake (~15 nm) was transferred over the device (method described in section 4.4.2). It permits to isolate the graphene heterostructure as well as the new contacts (Figure 4.19) from the top gates. Since the graphene heterostructure was defined as a bar, a pyramidal shape was defined in all its sides and as fabrication of the gates without the h-BN flake (or an insulator layer instead of), would lead to short the graphene and the top gates.

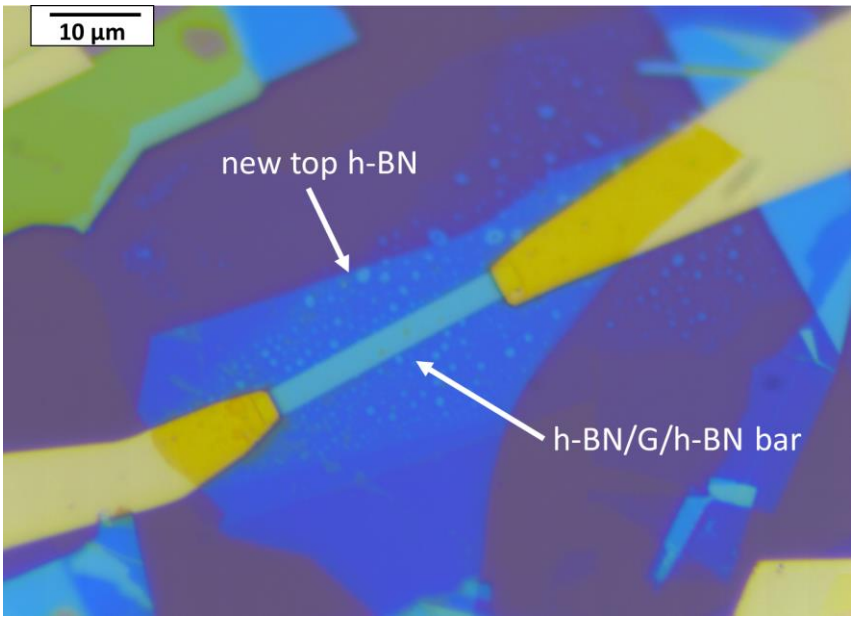
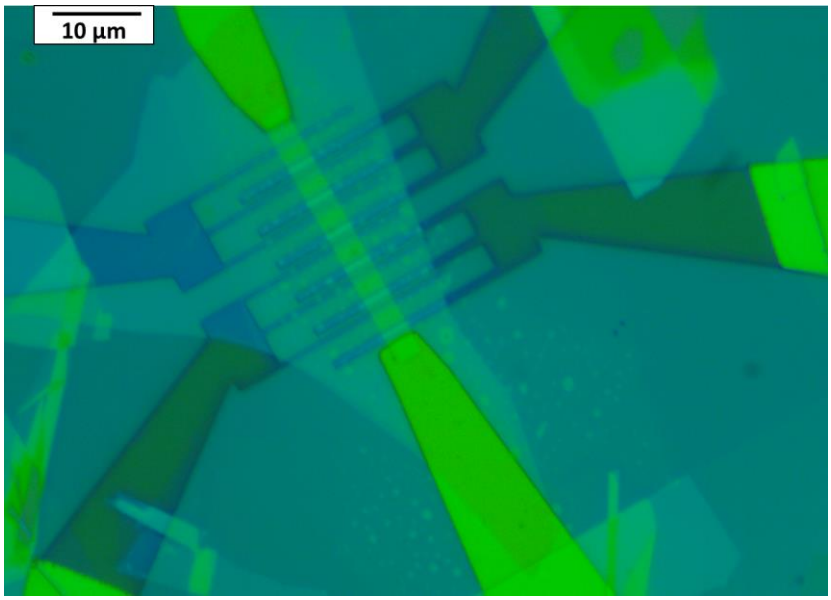


Figure 4.19 Optical image of the metalized Graphene heterostructure where a new top h-BN has been transfered.

7. Then, the sample was spin coated a third time and a third EBL was used to pattern the top gates contacts of the ADGG-GFET. The EBL used a dose of ~250 µC/cm2 for the top gates contacts (Figure 4.20 (a)).

8. After the development process, a second electron beam evaporation process of 15 nm Cr and 35 nm Au was performed for the top gates. Figure 4.20 (b) shows the final device with the Drain and Source edge metal contacts and the asymmetric top gates. To ease the lift-off process, every asymmetric top gate was defined as two different top gates with the same geometry and independent pads.

(a)



(b)

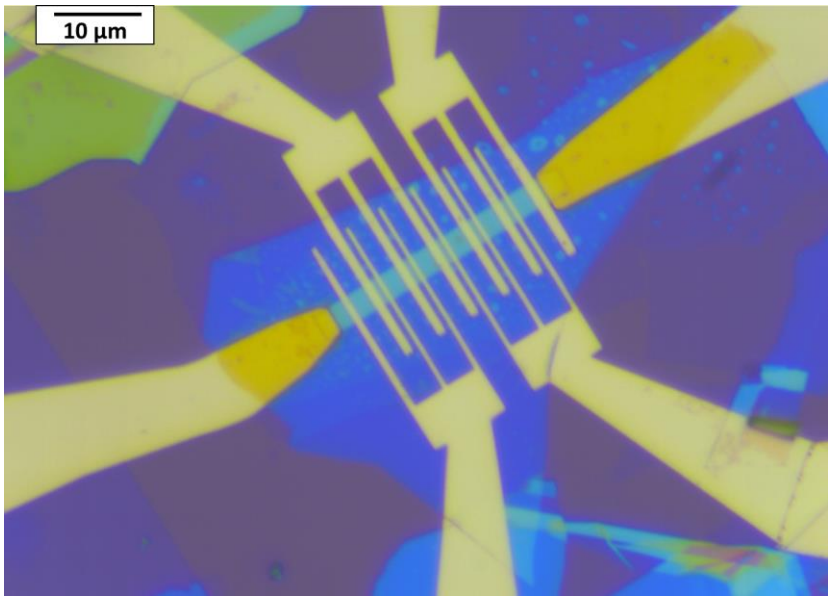


Figure 4.20 Optical image of the graphene heterostructure after the gates contacts has been patterned by e-beam lithography (a). The final ADGG-GFET after the asymmetric gates contacts were metalized (b).

The fabricated ADGG-GFETs were mounted on a DIL8 holder and glued with silver paste to allow the use of the back-gate contact. Finally, the device was wire-bonded and was electrically characterized.

4.4.4 Fabrication troubleshooting

The main problems faced during the fabrication process of the ADGG-GFETs and how they could be solved are presented below.

4.4.4.1 Production of large áreas

Usually, the mechanical exfoliation method leads to small areas of graphene or h-BN flakes. However, the fabrication of ADGG-GFETs requires large graphene flakes (>40 µm of length) and even larger h-BN flakes to ensure the complete encapsulation of the graphene sheet. As described in section 4.4.1 and proposed in [141], new steps were introduced. Prior to exfoliation, the SiO_2 substrate was cleaned with O_2 plasma as this would enhance the area of the subsequently exfoliated 2D material. Moreover, we found that a heat treatment at 100ºC during the exfoliation process and before peeling off the tape from the substrate may increase the size of the obtained area.

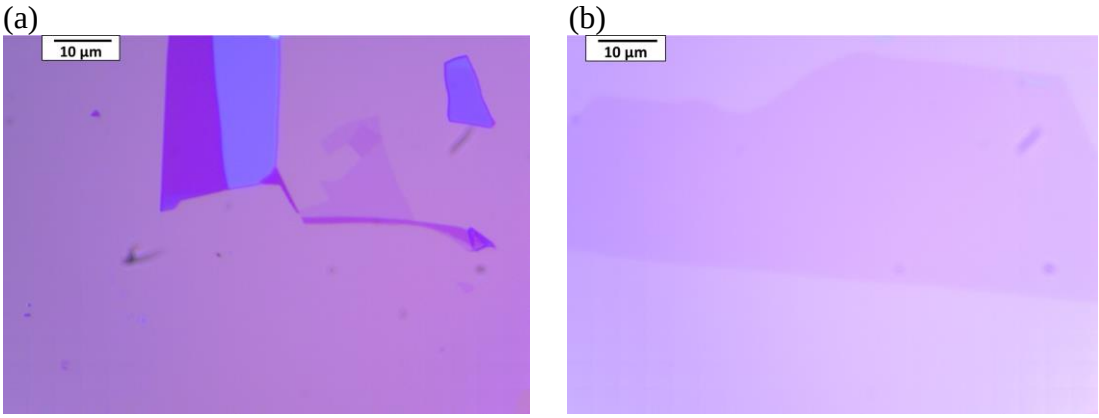


Figure 4.21 Optical images of Graphene flakes mechanically exfoliated without (a) and with (b) O_2 plasma cleaner treatment

Treatment with O_2 plasma enhances also the adhesion and the homogeneity of the graphene sheet (or other 2D material) as it could be observed in Figure 4.21. However, placing the graphene sheet directly on the Si/SiO_2 substrate drastically decreases carrier mobility [163]. To avoid this, the graphene flakes were transferred on h-BN flakes as the latter reduces the substrate interaction improving the carrier mobility (as it was described in section 4.4.2).

4.4.4.2 Graphene heterostructures fabrication

There are several problems coming out from the staking processes used to fabricate the graphene heterostructures. Namely, there are:

4.4.4.2.1 Emergence of blisters during transference

In the assembly of graphene and h-BN layers some blisters could appear at the interface of these materials as seen under the microscope (Figure 4.22). We observed that an excessive approaching speed and high temperature during the transference of the graphene and h-BN flakes lead to a high-density area of bubbles on the heterostructure inducing the set up of these blisters.

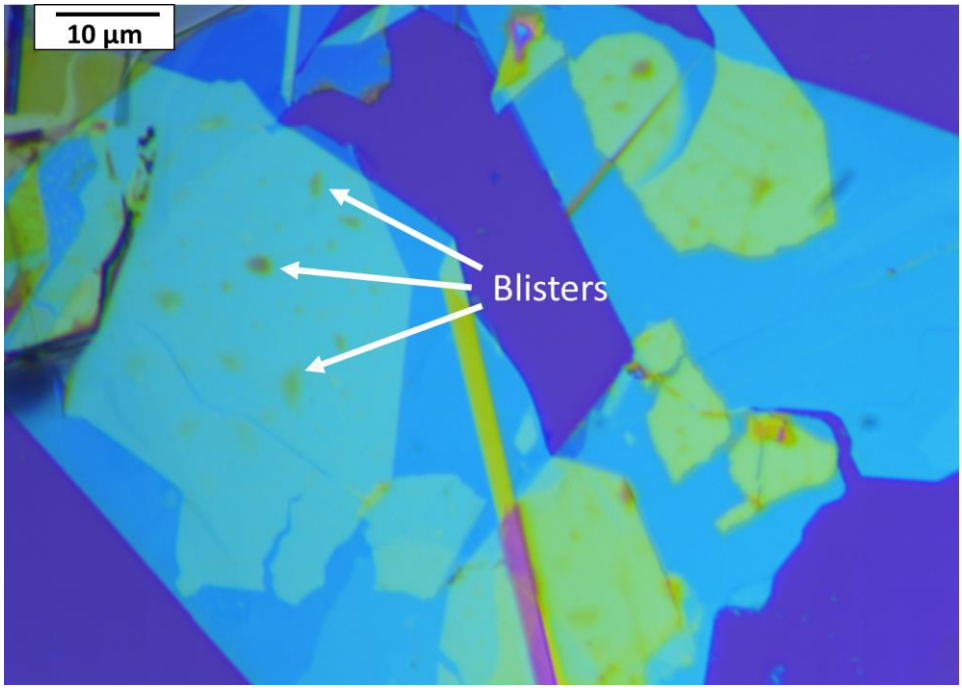


Figure 4.22 Optical image of a Graphene heterostructure with a high-density of blisters.

Figure 4.22 shows an example of h-BN/Graphene/h-BN heterostructure where an area with blisters is pointed. As we mentioned above annealing can help to remove these bubbles.

4.4.4.2.2 Heterostructures Breakdown

We also faced breaks of the flakes that were related to an excessive approaching speed as well as to high pressure leading to a lack of control of the assembly of heterostructures.

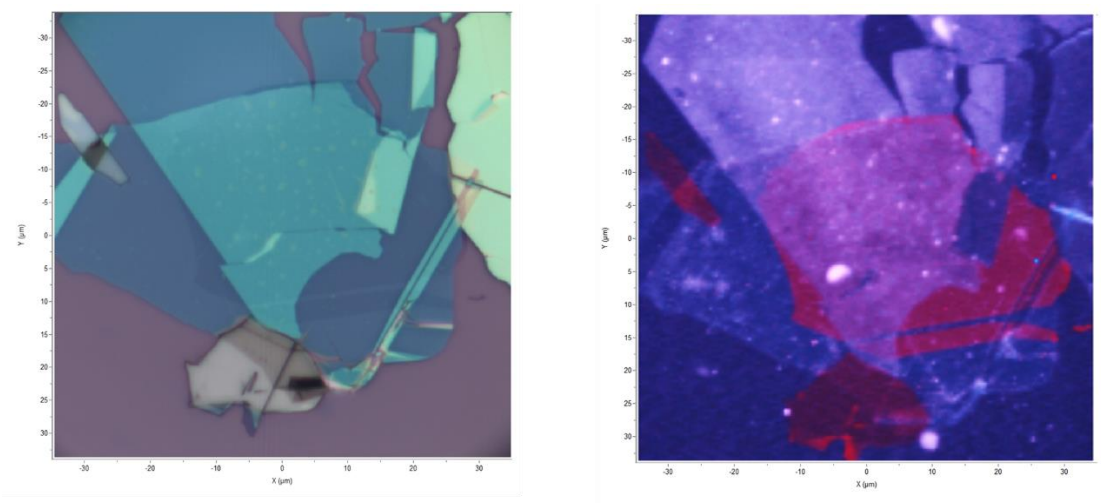


Figure 4.23 Optical (left) and false color Raman (b) images of a graphene heterostructure. The encapsulated graphene is highlighted in reddish color.

Figure 4.23 (left) shows the optical image of an h-BN/Bilayer graphene/h-BN heterostructure in which the heterostructure has been broken because of an excessive pressure applied during the transfer process. Furthermore, usually defects related to the transfer process are hard to be seen under the optical microscope. Raman mapping were performed to identify these internal defects. A key feature of Raman characterization is related to Raman imaging. By using an automatized XY stage, a pixel-by-pixel spectrum of the heterostructure can be acquired and then analyzed to generate false color image based on the material composition and structure (Figure 4.23 (Right)).

4.4.4.2.3 Detach process failures

Finally, another problem could emerge from picking up or detach the graphene, the h-BN, or the whole heterostructure, from the Si/SiO_2 substrate. Excessive temperature during the peeling-off could lead to a low density of detached flakes. Temperature shortage turns the PPC crystalline leading automatically to the breakage of the flakes. Moreover, graphene exfoliated using O_2 plasma treatment shows higher adherence to the substrate and, thus, the transference processes is hindered.

To overcome this problem, the h-BN/graphene heterostructure was immersed into acetone for at least 2 hours and then the transfer method was repeated. We found that after this treatment the adhesion between the graphene layer and the substrate interface was weakened and then the detachment process was easier.

4.4.4.3 High quality edge contacts

A key feature in this graphene FETs fabrication is the development of the quasi one-dimensional contacts to define the source and drain ohmic contacts. We optimized the SF_6/O_2 plasma RIE recipe to get a pyramidal shape on the graphene heterostructure, this shape is helpful to place such contacts. A non-adequate recipe would lead to a non-

uniform shape on the lateral face and consequently a non-adequate drain or souce contacts (Figure 4.24).

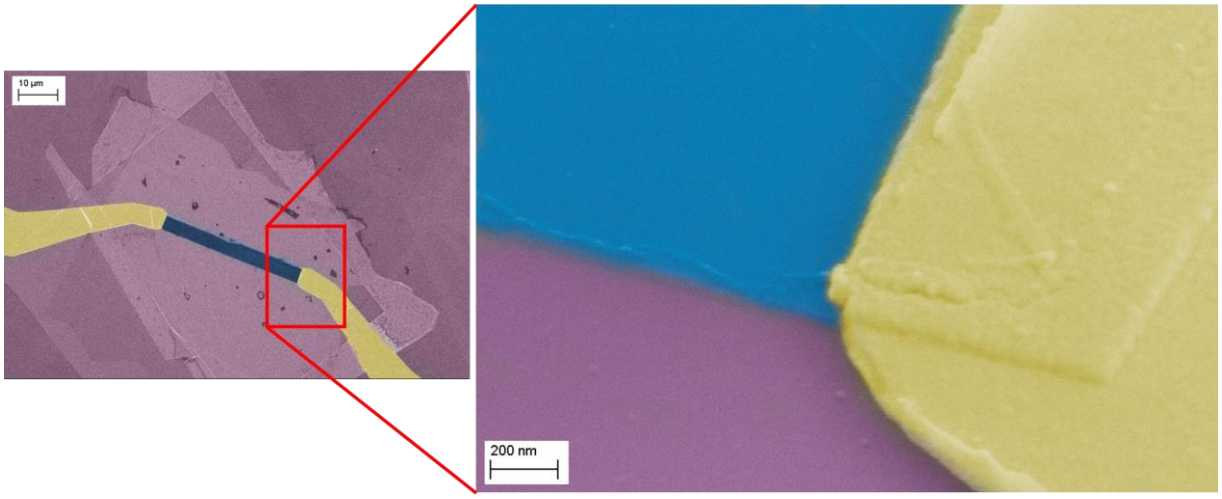


Figure 4.24 False color SEM image of a graphene heterostructure. The graphene is completely encapsulated between two flakes of h-BN. Legend color is as follows: h-BN (blue color), metal (yellowish color) and $SiSiO_2$ substrate (purple color).

We observed that low evaporation rates, especially of Cr, enhance the junction between the Graphene and the Cr/Au metal layers as they ensure higher homogeneity, lower roughness and excellent control of the thin film evaporation (< 10 nm). However, high evaporation rates create non-homogeneous films leading to a low quality or absence of junction between graphene and the Cr/Au metal film.

4.4.4.4 Lift-off problems

One of the latest issues may appear during or after the lift-off process. There are several reasons that can lead to a failed lift-off process and subsequently a failed ADGG-GFET fabrication. As the adhesion between the Cr/Au film and h-BN is not excellent, an excessive flow pressure of acetone applied with the syringe could detach the top gates fingers from the top h-BN flake (Figure 4.25).

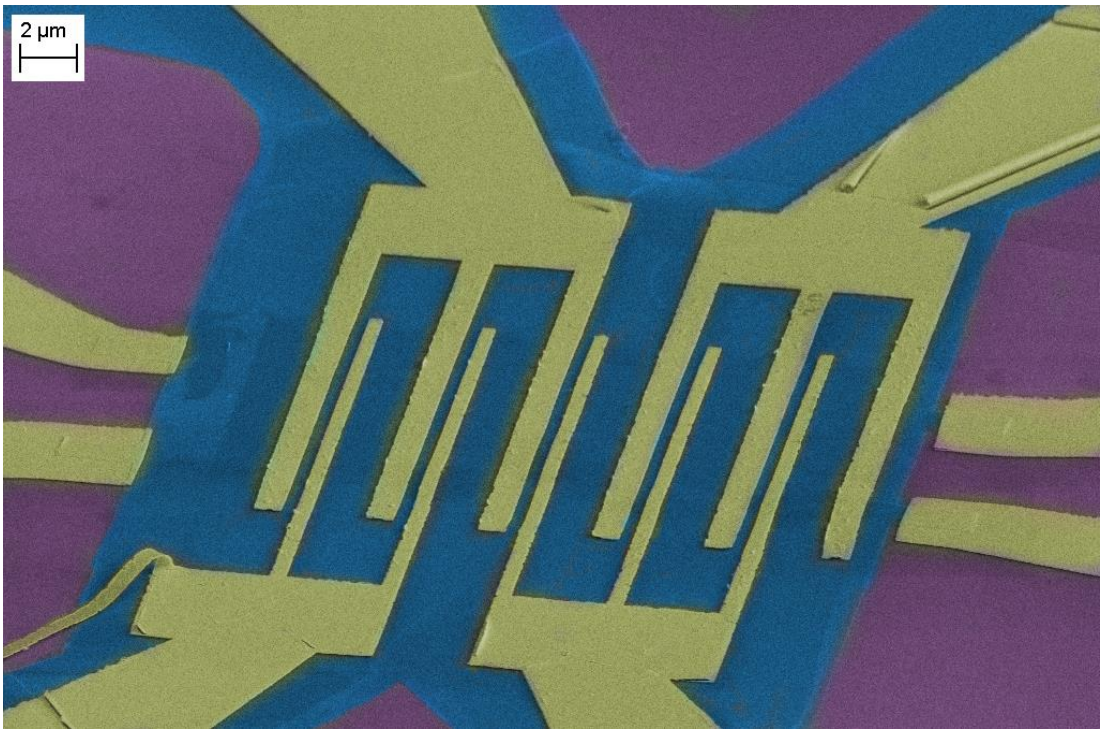


Figure 4.25 False color tilted SEM image of an ADGG-GFET which has a finger bent and a delamination problem.

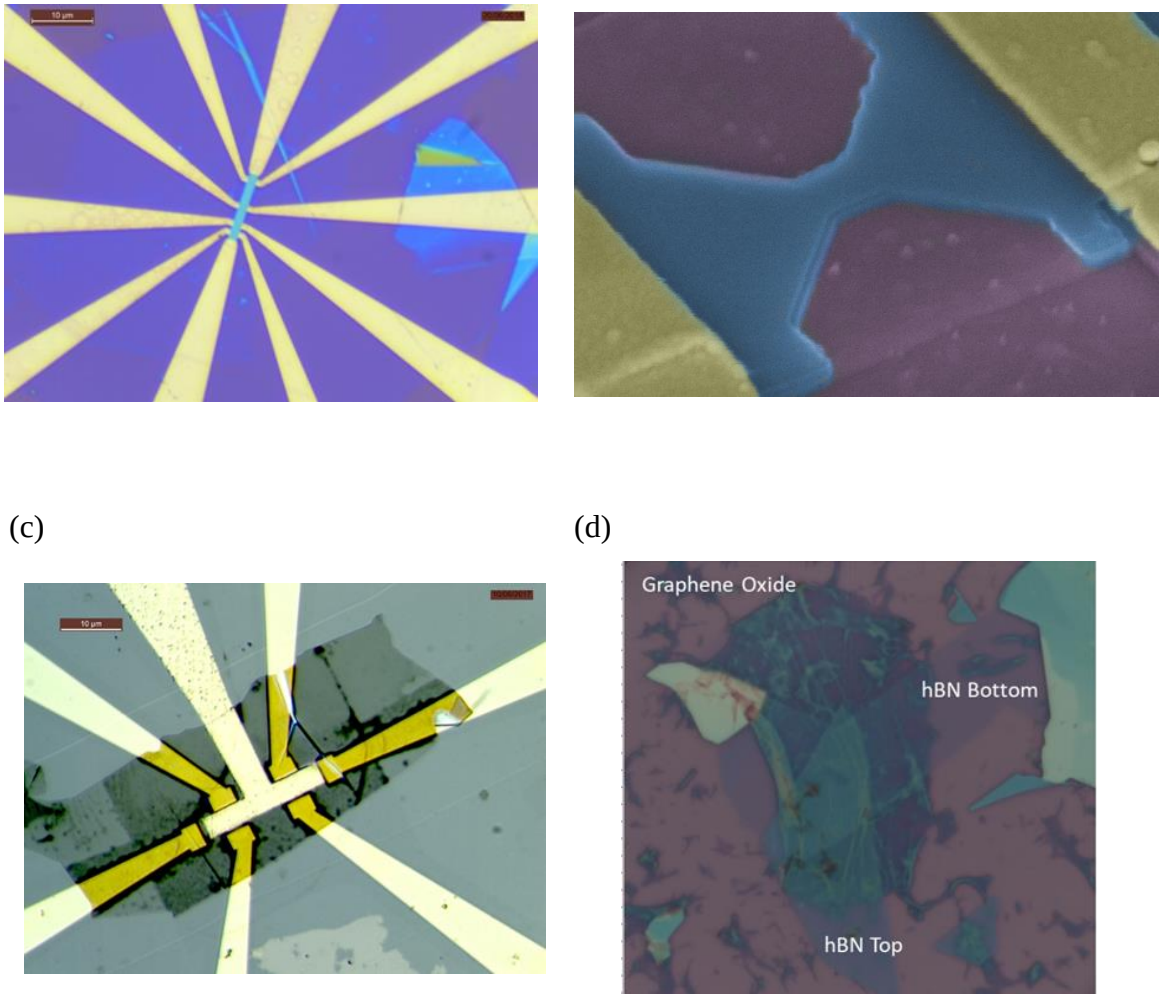
Moreover, as we mentioned above, high evaporation rates decrease the homogeneity of the metal film as well as the quality of the junction leading to a delamination of the metals. Both problems can be observed on Figure 4.25.

Furthermore, additional issues related to the cross-linking of the resist during the e-beam evaporation may arise. The subsequent lift-off processes become difficult or impossible. As the evaporation is done by an e-beam gun and the resist is sensitive to electrons, we found that placing the sample in a specific region on the chamber during the evaporation leads to an electron overdose on the resist by the electrons reflected from the metal placed on the liner and thus cross-linking the resist.

4.4.5 Beyond ADGG-GFETs

In parallel to the development of the ADGG-GFET, the heterostructure h-BN/Gr/h-BN was also used for fundamental physics studies. Figure 4.26 (a) shows a h-BN/Gr/h-BN hall bar which was used to characterize electrically this type of structure and hence extract the carrier mobility and density. Figure 4.26 (b) shows a h-BN/G/h-BN heterostructure with a 200 nm nanoconstriction that was measured to observe the quantized conductance at low temperature.

(a) (b)



(c) (d)

Figure 4.26 Optical or SEM images of different graphene based heterostructures. Hall-bar (a) and nanocontriction (b) graphene heterostructures. Epitaxial hall bar heterostructure with a top gate (c). Graphene oxide heterostructure (d).

Even if our main research line in this PhD work was dedicated to the study and use of exfoliated graphene, we fabricated and partially studied other graphene-based technologies. Figure 4.26 (c) shows an epitaxial graphene hall bar in which a h-BN flake was transferred on it in order to fabricate a top Gate. Another graphene based heterostructure consists on a h-BN/Graphene oxide/h-BN heterostructure showed on Figure 4.26 (d) employed to study the behavior of the Graphene Oxide when it is encapsulated; the properties of the structure and its applications as gas sensor were explored.

4.5 Results and discussion

The fabricated devices were characterized electrically by measurements of the output chacteristics and the charge neutrality point (or Dirac point). It was also subjected to terahertz radiation at two freuqnecies 0.15 and 0.3 THz. The measurements were performed at different temperatures from 4K up to 300K. To demonstrate its importance for terahertz technology, the device was used as a sensor in a THz imaging and inspection of hidden object was demonstrated.

4.5.1 Electrical characterization at low temperature

Figure 4.27 (a) shows the Asymmetric-Dual-Grating-Gate Graphene Field Effect Transistor (ADGG-GFET) characterized in this chapter. The geometrical parameters of the grating are: L_{G1}=500 nm, L_{G2}=1 µm, d_1=1.5 µm, d_2=3µm, s_1=1µm and s_2=1.5µm. The ADGG-GFET was cooled down to 4 K and placed on the optical cryostat described on section 2.1.

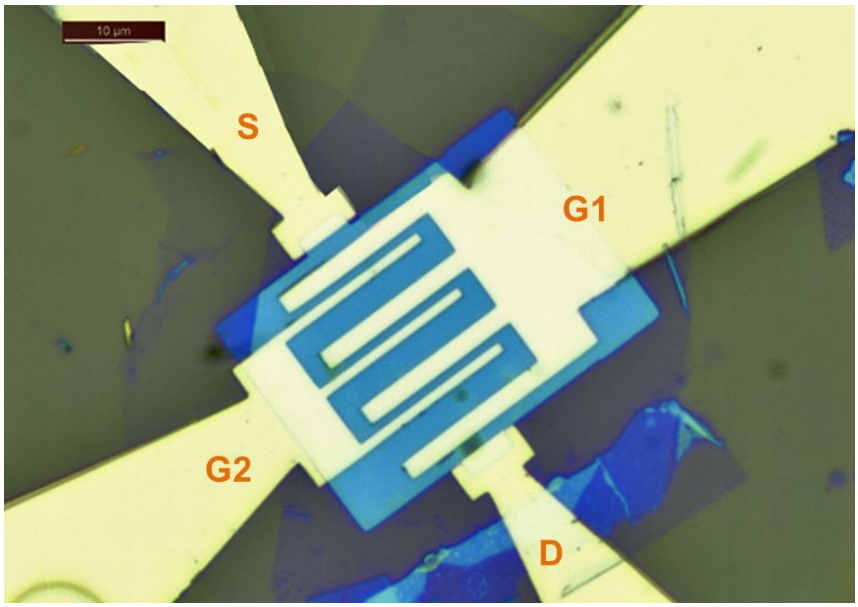


Figure 4.27 Optical image of the ADGG-GFET under studio on this section. The drain (D), source (S) and gates (G1, G2) are highlighted.

Figure 4.28 shows the drain-to source current (I_{DS}) as a function of the drain-to-source voltage bias (V_{DS}) of the ADGG-GFET. Measurements were performed at room temperature, in absence of voltage bias applied to the gates (back and top gates) using a Keithley 2412A sourcemeter. The device showed an excellent linear dependence with V_{DS} in the range (-100 mV to 100 mV) demonstrating the excellent ohmic behavior of the contacts made by Chromium and Gold as metallic edge contacts [160]. An equivalent resistance of 2.6 kΩ was extracted from measurements that corresponds to a serial resistance of the two edge contacts (Drain and Source) and the graphene channel.

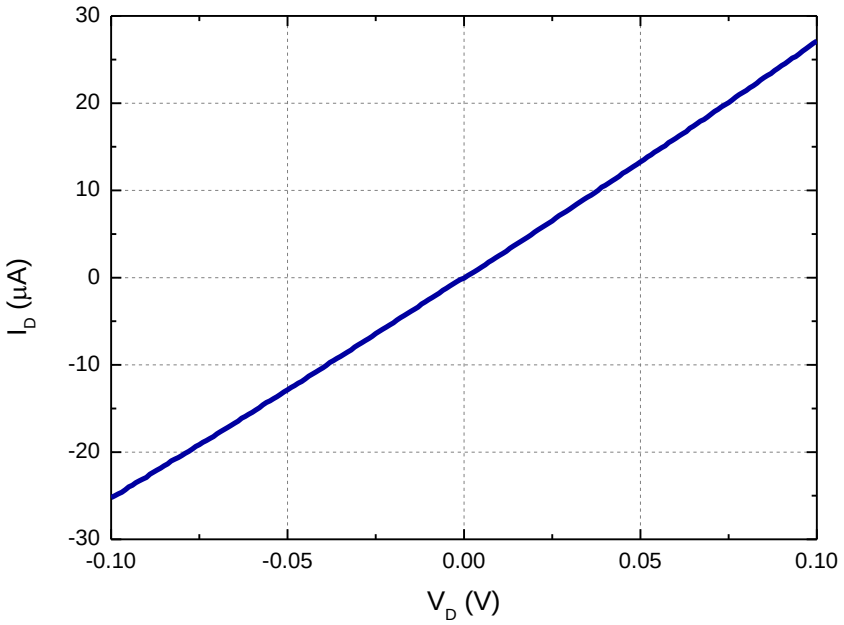


Figure 4.28 Drain-to-source current vs drain-to-source voltage of the ADGG-GFET. The linear behavior obtained showed an ohmic conection.

The charge neutrality point (CNP) was measured using a standard lock-in technique [164]. An AC sinusoidal signal with frequency around 11 Hz and rms amplitude of 1V was applied to the channel through a high value resistor of 100 MΩ. This setup allows the injection of a constant 10 nA current intensity since the channel resistance (few kΩ) is much lower than the 100 MΩ resistor connected in series. Figure 4.29 describe schematically the setup used in the CNP measurements. Two lock-in amplifiers were used. The first one was dedicated to measure the intensity of the current and the second one to measure the V_{ds} voltage drop across the channel as a function of the gates (top or back gates) voltage. Different sourcemeters were used for the back and top gates. At $V_{bg}=V_{g1}=V_{g2}=0$ V, the drop voltage between drain and source was around 25.6 μV which gives a resistance of 2.56 kΩ, in agreement with the value obtained previously using the sourcemeter.

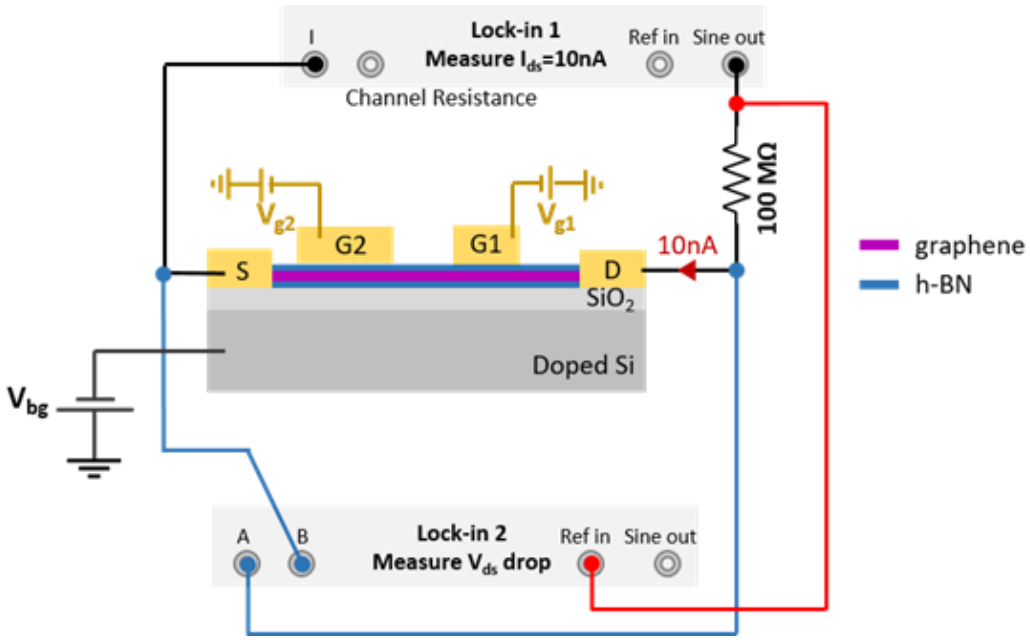


Figure 4.29 Schematic representations of the configuration used to perform current and voltage measurements on the ADGG-GFET device using the Lock-in Amplifier technique.

Figure 4.30 shows the obtained CNP results for the transistor as a function of the back gate (a) and top gate (b) voltages for different temperatures in the range (4K-300 K). The channel resistance shows a typical "bell" shape when the back gate bias is varied [138]. With negative back-gate bias majority carriers are holes. Increasing the gate bias, the measured resistance increases and reaches its maximum at the CNP (called also Dirac point). The CNP indicates the level of Fermi energy, where valence and conduction bands are in contact. Since graphene is a gapless material, the transistor cannot be switched-off like a normal transistor. For positive back-gate voltage, majority carriers are electrons. As shown in Figure 4.30, the CNP was reached for a value of the back-gate voltage around $V_{BACK\text{-}GATE}$=-5.8V indicating that the graphene sheet was non-intentionally n-doped.

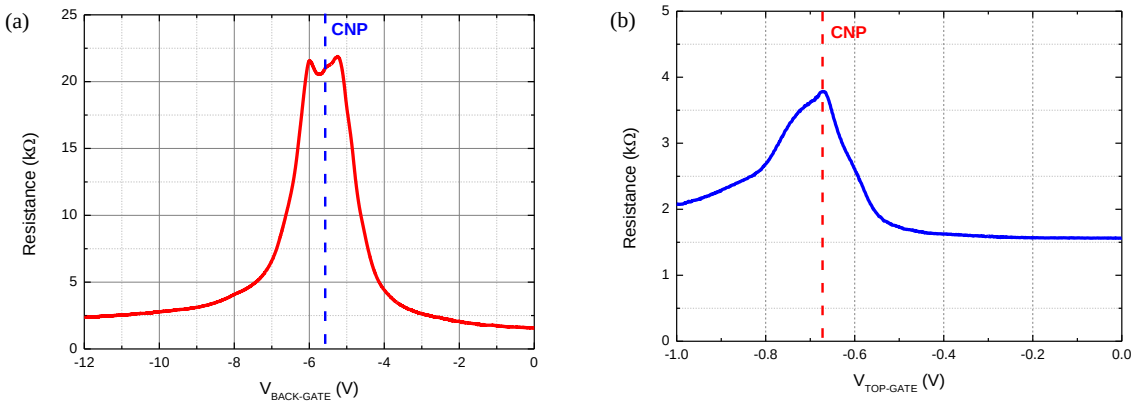


Figure 4.30 Channel resistance as function of the Back-gate (a) and top-gate (b) voltages at 4.2 K

The resistance of the ADGG-GFET (Figure 4.30) exhibit a different shape with two distinct peaks that suggest a different behavior as compared to the observed in the forme study of a single gate device. This effect could be attributed to superposition of different doping profiles, and hence conductivity, beneath the gates fingers (G1 & G2) as well as in thw ungated region which are affected by the back gate. The built-in voltage under the metal fingers of the gate could introduce the doping of the graphene sheet. A first approach is to describe the global resistance of the channel as the series of three partial resistences:

$$R\left(V_{BG},V_{TG1},V_{TG2}\right)=R_1\left(V_{BG},V_{TG1}\right)+R_2\left(V_{BG},V_{TG2}\right)+R_3\left(V_{BG}\right) \quad \textbf{(4.1)}$$

The first and second terms (R_1 and R_2) of equation 4.1 are related to the top gate fingers of G1 and G2, respectively. Since the back-gate covers the whole channel, it also affects those terms. The third term (R3) is only a function of the back gate since it's related to the (upper) ungated parts of the channel. The obtained result at 4K was fitted by those three functions and the result is shown in Figure 4.31.

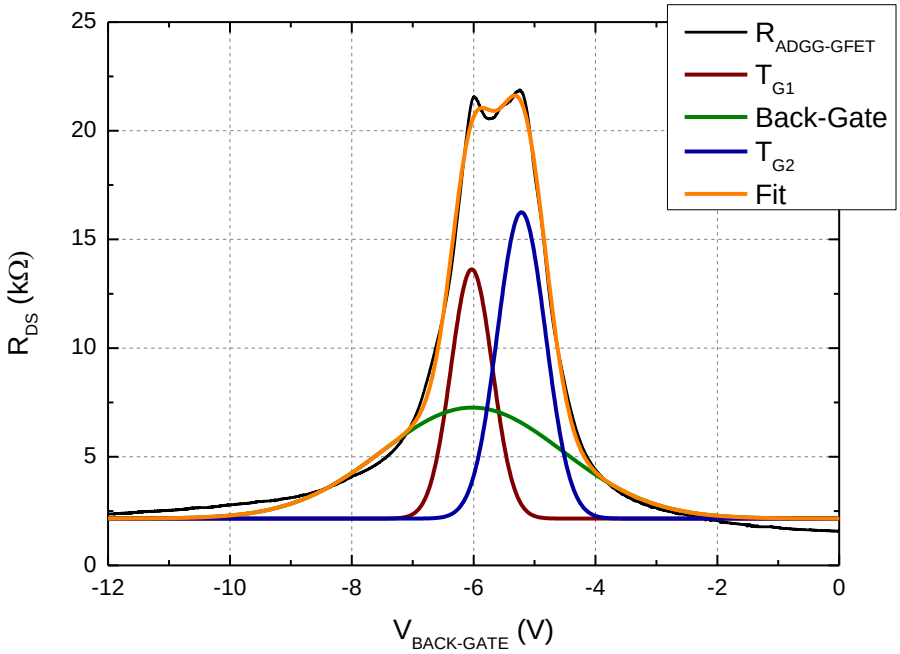


Figure 4.31 Channel resistance as function of the back-gate voltage at 4.2 K in black color and the fitted curve in orange color. Red, green and blue curves represent the deconvolved curves.

Usually a model is used to extract the carrier mobility and density from the measured CNP [165]. The total resistance is given by the equation 4.2 [166]:

$$R_{tot} = R_c + R_{channel} = R_c + \frac{N_{sq}}{n_{tot} e \mu} \tag{4.2}$$

where R_c represent the contact resistance, R_{ch} the channel resistance, N_{sq} is the number of squares in the graphene channel (the length over width ratio), e is the absolute value of the elementary charge and, μ is the field effect mobility. The total charge carrier concentration n_{tot} can be approximated as $n_{tot} = \sqrt{n_0^2 + n^2}$, where n_0 is the residual charge carrier concentration and n is the carrier concentration induced by the back-gate given by:

$$n = \frac{C_{ox}}{e}(V - V_{CNP}) \tag{4.3}$$

where V_{CNP} is the gate voltage at which the charge neutrality point appears, and C_{ox} is the gate oxide capacitance per unit area. This expression for N_{tot} is then inserted back in Equation (4.2) to obtain:

$$R_{tot} = R_c + \frac{N_{sq}}{\sqrt{n_0^2 + n^2}\, e\mu} \tag{4.4}$$

The three parameters of equation (4.4) n_0, μ and R_C are used to fit the measured data (R_{tot}). The resistance was fitted to the experimental data points around the charge neutrality point (V_{CNP} = -5.5 V) to extract the three parameters. The measurements corresponding to the hole and electron branches of the measurements were independently fitted to determine the contact resistance and hole/electron carrier mobilities.

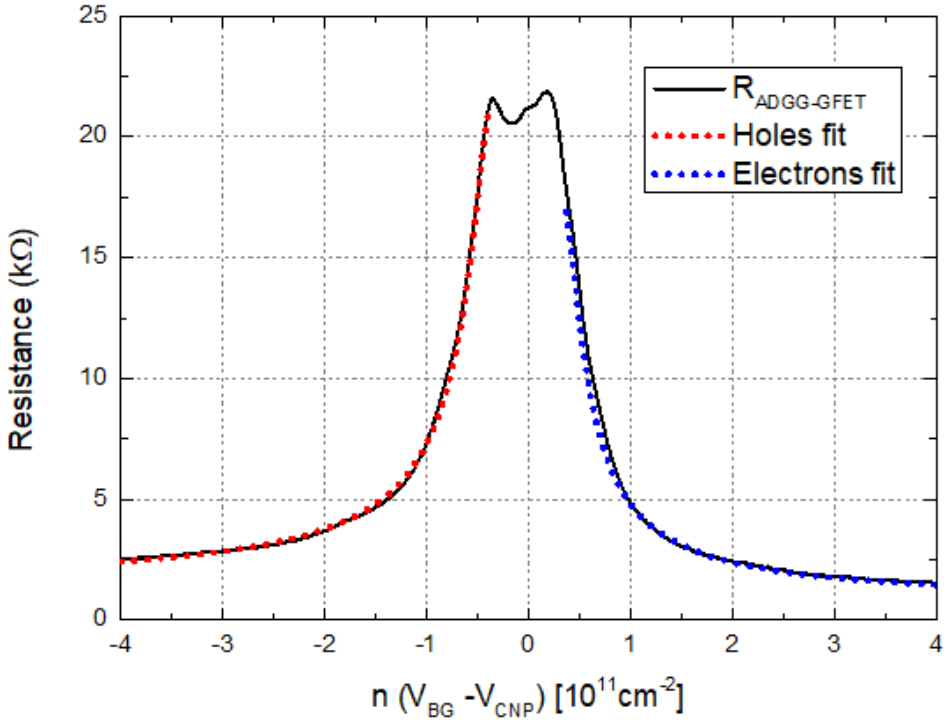


Figure 4.32 Experimental data of the channel resistance as function of the back-gate voltage at 4.2 K and the fitted electron (blue) and (hole) branches.

Figure 4.32 shows the experimental data (solid line) at 4K and the fiting functions for hole (red circle) and electron (blue circle). Hole and electron carrier mobilities were estimated from the fitting results as μ_e = 150589 $cm^2V^{-1}s^{-1}$ and μ_h = 108476 $cm^2V^{-1}s^{-1}$. These excellent values of carrier mobilities are in agreement with the Raman measurements presented in section 4.4.2 which showed a high intensity I2D/IG ratio (around 8) on the graphene heterostructures prior to processing. Moreover, the extracted

values for carrier mobilities show that the ADGG-GFET is a competitive device in terms of channel mobility as compared to state-of-art semiconductor technology [167] as well as to non-encapsulated graphene FETs [168]. This must be attributed to the excellent properties of encapsulated graphene. Ohmic contact resistances were estimated to R_C = 992.6 ± 316.4 Ω that is an admissible value considering that drain and source were defined as quasi-one-dimensional contacts.

4.5.2 THz detection measurements at low temperature

The ADGG-GFET was cooled down to 4 K and subjected to terahertz radiation at two frequencies (0.15 & 0.3 THz). In this case, no DC current was applied to the channel of the device. The THz beam was collimated and focused on the ADGG-GFET by a parabolic mirror and an optical lens (Figure 2.1). The photocurrent generated by the THz radiation was measured on the drain contact by the lock-in Amplifier while the source contact was grounded. The THz beam was modulated by a mechanical chopper at 233 Hz used as a reference for the lock-in amplifier. More information about the experimental setup can be found on Section 2.1.

Figure 4.33 shows the obtained photocurrent signal when the ADGG-GFET was excited with 0.15THz (blue) and 0.3THz (red) EM radiation. The intensity of the signal measured at 0.15 THz was much lower and, for the sake of clarity and comparison, it was multiplied by factor 20. The device exhibits a clear photocurrent under both excitation frequencies. A maximum of photocurrent around 1.5 nA was measured for $V_{BACK\text{-}GATE}$=-5.2V, close to the CNP and under an excitation of 0.3 THz. The photocurrent obtained under excitation at 0.15 THz was much lower than for 0.3 THz because the inefficient coupling of the THz radiation with the structure at lower frequencies. It was demonstrated that the metallic contact is better for coupling the radiation at higher frequencies [70], [84]. The behaviour of both signals when the back-gate bias is vaied is similar and repetitive at both frequencies.

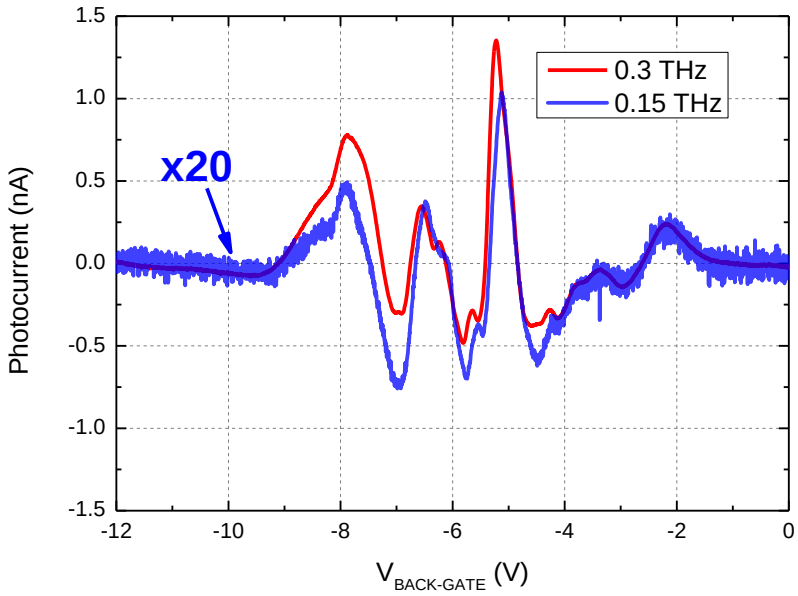


Figure 4.33 Photocurrent obtained as function of the back-gate voltage at 4.2 K when the device was illuminated at 0.15 (blue) and 0.3 (red) THz. The 0.15 THz curve is multiplied by a factor 20.

THz radiation was modulated by the mechanical chopper at 0.33 kHz and then foucused into the device. The maximum experimental photoresponse as well as on strained-Si MODFETs remained unchanged over the chopper frequency range 0.1-4 kHz demostrating the fast response (0.2 ms or higher) of THz detection.

As we mentioned in Chapter 1, the main detection mechanism of terahertz radiation on gated-FETs is based on nonlinear properties of the two-dimensional electron (or hole in p-channel devices) plasma in the sub-micron channel of a field-effect transistor. Non-resonant detection is observed when $\omega\tau < 1$ where ω is the angular frequency and τ the scattering time $(\tau \sim \mu m^*/e)$ that results in momentum relaxation. The effective cyclotron mass of the charge carriers is given by $(m^* = \hbar k_F v_F)$ where v_F is the Fermi velocity with typical values ~10^6 m/s and the Fermi momentum $k_F = \sqrt{\pi n}$. The charge carrier concentration is given by Equation 4.3. The gate oxide capacitance per unit area (C_{ox}) is given by $\varepsilon_r \varepsilon_0 / t_{ox}$ where ε_r is approximately 4 for SiO_2 and h-BN and t_{ox} is the oxide thickness equal to 310 nm (295 nm for SiO_2 and 15 nm for h-BN). The scattering time was found around 0.3 ps and at the higher frequency (0.3 THz), $\omega\tau \sim 0.7$ at 4K. Under such condition, only non-resonant detection could be observed. However, the obtained quality factor $(\omega\tau)$ is close to one and could be increased either by a better graphene sheet (with higher carrier mobility), orby increasing the excitation frequency.

Although Dyakonov and Shur mechanism is the main recognized mechanism for FET THz detection, additional effects may be involved in the photoresponse when a GFET is employed as a THz detector. For example, the photo-thermoelectric effect (PTE)

arising from the temperature gradient in a FET can contribute to the photoresponse [[169]]. Nevertheless, both PTE and Dyakonov and Shur mechanims exhibit a similar dependence on the gate voltage and, as result, it is challenging to discern the origin of the observed rectification [[170]]. Both mechanisms can be described as follows:

$$\Delta U \sim \frac{1}{\sigma}\frac{d\sigma}{dV_G} \tag{4.5}$$

This model yields a photovoltage ΔU proportional to the derivative of the channel conductivity with respect to the gate bias. As the main results obtained in the measurements of ADGG-GFET as THz photodetectors were related to the photocurrent generated, the expression (4.5) can be appropriately modified to predict the photocurrent generated. Photovoltage and photocurrent generated by an external THz field are directly related, [171], by the Ohm´s law as:

$$\Delta U = R \cdot \Delta I \tag{4.6}$$

Where R is the ADGG-GFET resistance previously measured (Figure 4.29). Using equation (4.6) and $R \approx \frac{1}{\sigma}$ into equation (4.5), it can be rewritten as:

$$\Delta I \sim \frac{d\sigma}{dV_G} \tag{4.7}$$

Equation (4.7) shows that the photocurrent generated between drain and source terminals is proportional to the derivative of the device conductance with respect to the gate bias. Figure 4.34 shows the predicted photocurrent at low temperature as a function of the back gate.

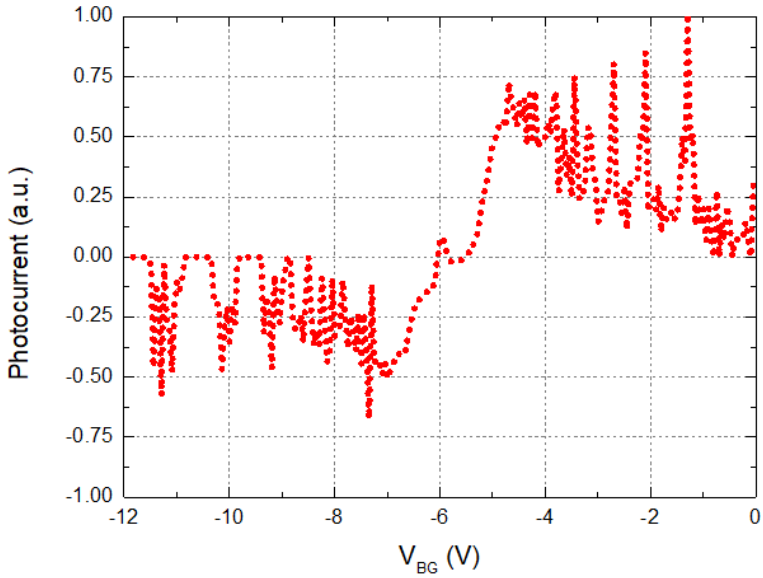


Figure 4.34 Calculated photoresponse of the ADGG-GFET as function of the back-gate voltage.

The predicted photocurrent (ΔI) varies from negative to positive values, while crossing the CNP; this is consistent with the ambipolar nature of charge carrier transport in graphene [92]. Two maximum peaks can be observed; a positive peak photocurrent at -4.5V gate-to-source voltage and a negative peak photocurrent around -7V in agreement with the experimental measurements. Between these two peaks a fluctuating behavior can be observed, as it is found in measurements. Beyond these two peaks, the predicted photocurrent generated becomes noisier as consequence of the limited resolution of the equipment on the CNP measurements (Figure 4.30 (a)) making it imposible to analyze the measurements. Nevertheless, the fluctuating behavior of measurement results can be explained as the global sample resistance that is determined by the contribution of the three resistances (Equation 4.1). Then, the photocurrent (ΔI) can be rewritten as showed in equation (4.8):

$$\Delta I \sim \frac{d\sigma\left(V_{BG},V_{TG1},V_{TG2}\right)}{dV_{BG}} = \frac{d\left(1/R\left(V_{BG},V_{TG1},V_{TG2}\right)\right)}{dV_{BG}} \qquad \textbf{(4.8)}$$

Therefore, the photocurrent is due to the contribution of the three resistances as plotted in Figure 4.35:

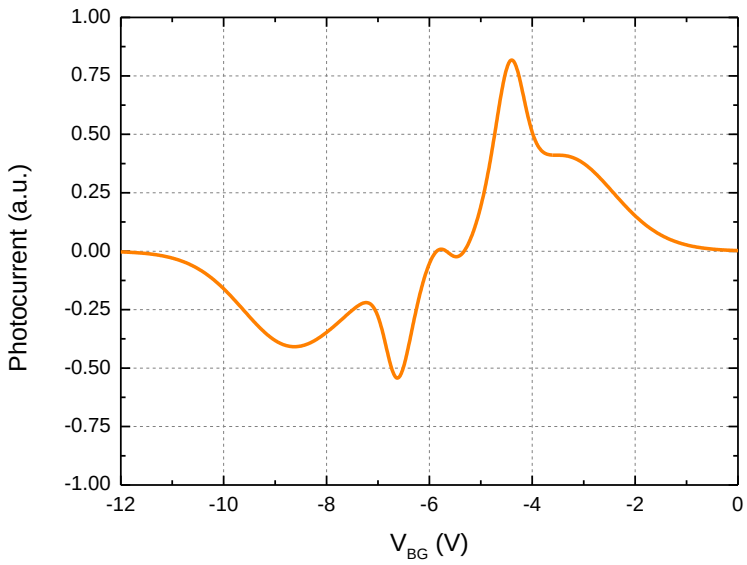


Figure 4.35 Calculated photoresponse obtained from the fitted channel resistance as funciton of the back-gate.

Equation (4.8), and therefore the photocurrent showed in Figure 4.35, is only an approximation of the photocurrent obtained from the 2-probes resistance fit and it only approximates the behavior of the photocurrent. External factors could also strongly affect the device behavior: coupling of the THz radiation with the device, blisters causing unexpected non-uniform doping, ..., that may be at the origin of the observed discrepancies. Nevertheless, the most intense peaks experimentally obtained are predicted in Figure 4.35. Sign difference between experimental and theoretical comes from the match phasing of the lock-in amplifier in measurments.

Figure 4.36 shows the temporal behavior of the photocurrent signal when the THz radiation was switched ON and OFF at both frequencies (a) 0.3THz (b) 0.15THz. The back-gate voltage was fixed around -5.2V at which maximum intensity of the measured signal was observed (Figure 4.33)

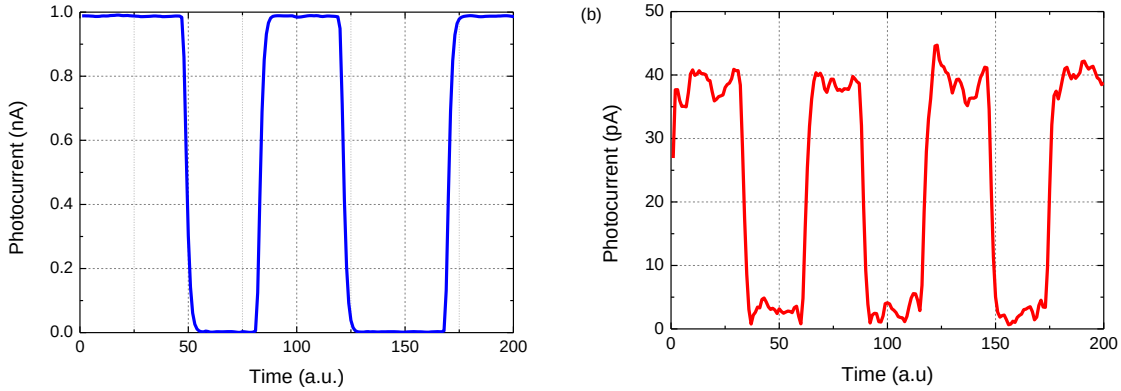


Figure 4.36 Photocurrent generated as function of the time at 0.3 (a) and 0.15 (b) THz when the THz radiation was switched ON and OFF.

From Figure 4.36 it is evident that the Graphene FET recovers rapidly the original photocurrent when the THz light is switched ON and OFF. The rise and decay times of the ADGG-GFET ON-OFF states were below the equipment detection limit, which was lower than 100 ms. The signal observed under 0.3THz excitation was considerably more intense (20 times higher) than the one obtained under excitation at 0.15THz. It also shows better Signal-to-noise ratio (SN). As we mentioned on section 4.3, the potential of the Asymmetric Dual Grating Gates lies on the tunability of the response on the THz regime. After considering the results of measurements under 0.15 and 0.3 THz at low temperature, the ADGG-GFET configuration studied in this section seems to exhibit a behavior more adequate for the higher frequencies in the sub-THz/THz range. Nevertheless, the lack of sources of higher frequencies in our laboratory, made it impossible to perform additional measurements.

Henceforth, only measurements at 0.3 THz were realized because as the THz source must be displaced and realigned when it is switched from 0.15 THz to 0.3 THz the excitation conditions would vary between the two frequencies.

Photocurrent signal was also measured as a function of the biasin of the top gates and for V_{BG}=0V (Figure 4.37 (a)). A maximum photocurrent close to 1nA was found.

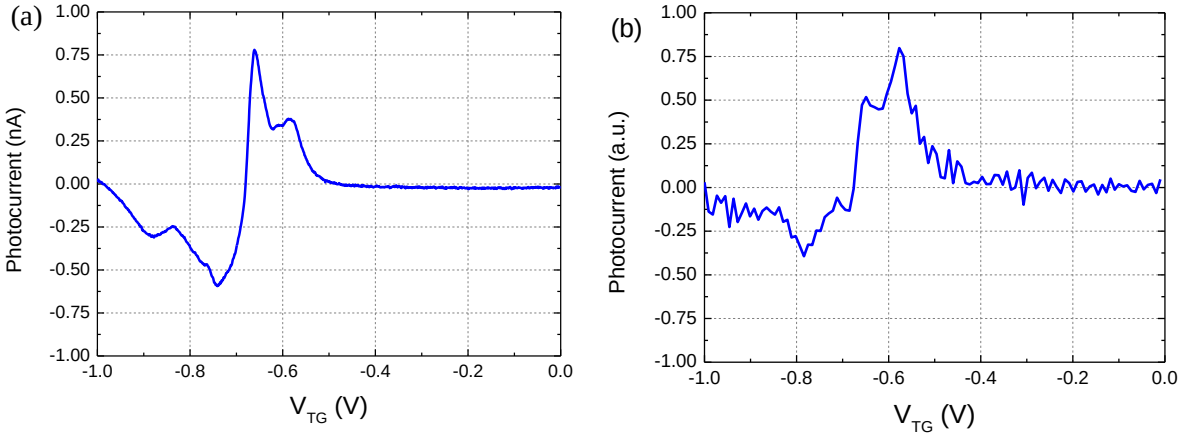


Figure 4.37 Experimental photocurrent as function of the Top Gate voltage at 4.2K when the device was illuminated at 0.3 THz (a) and the calculated photocurrent (b).

The obtained results are comparable to the ones measured in a single gate transistor [92], [171] when it pass from positive to negative values at the CNP position around V_{TG} = - 0.7 V. The influence of the other top gate as well as the back gate can be observed on the fluctuations beyond the CNP around -0.6 V and -0.8 V. The behavior observed in experimental measurements at 0.3 THz (Figure 4.37 (a)) is in agreement with the predictions obtained from the CNP and showed in Figure 4.37 (b). The predicted photocurrent exhibits the same dependence and two maximum positive peaks close to V_{TG}=-0.7V and V_{TG} -0.58V were found along with an additional negative peak for a value of V_{TG} close to -0.8V as experimental photocurrent.

We found that the photocurrent generated can be improved by biasing both top and back gates. Previous measurements only showed the photocurrent generated when the ADGG-GFET was biased either with the back-gate or the top gate.

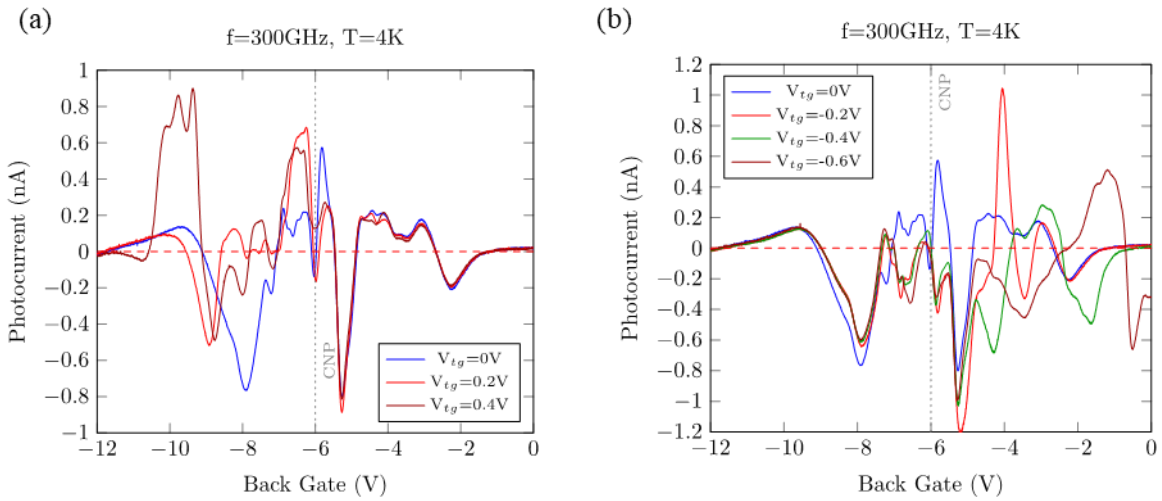


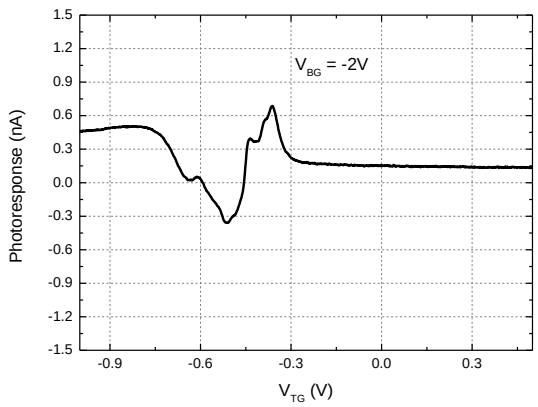
Figure 4.38 Photocurrent generated as function of the Back-Gate voltage at 4.2K and 0.3 THz

when the device was polarized at positive (left) and negative (right) voltages.

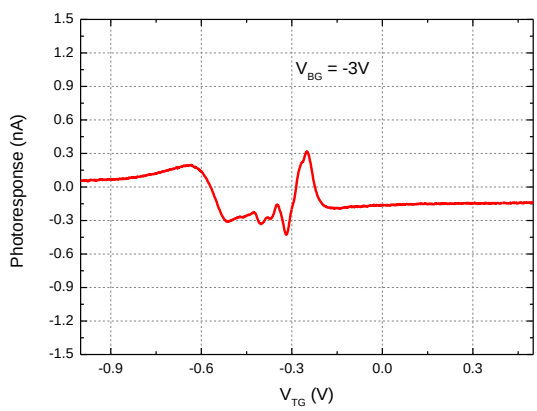
Figure 4.38 shows the photocurrent generated by the ADGG-GFET vs the back-gate voltage at 0.3 THz while the top gate was biased at different positive (a) and negative (b) voltages. The photocurrent generated can be enhanced by biasing both top and back gates. We found that positive values of top gate voltage mostly affect the left side of the CNP. In the one hand, negative top gate voltages only affect the right side of the CNP. This effect can be understood by considering that the two top gates are independently biased. The application of a voltage to one of the top gates will essentially modify the contribution to the global channel resistance associated to this gate (R1 or R2). When the top gate is biased with negative voltages, this resistance contribution is displaced to positive values while keeping essentially unmodified the other ones while modifying the total resistance [165] of the device and, thus, the generated photocurrent. In the other hand, similarly to the above, when the top gate is biased at positive voltages, this resistance contribution is displaced to negative values modifying only the photocurrent generated on that side.

Moreover, Figure 4.39 (a) shows the experimental values of the photocurrent measured experimentally at 0.3 THz and 4K vs the top gate voltage when the ADGG-GFET is biased under different back-gate voltages.

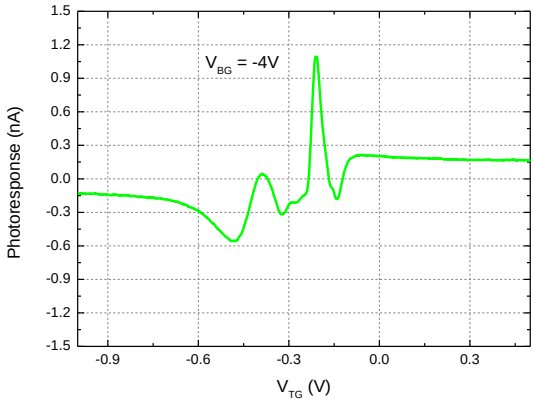
(a)



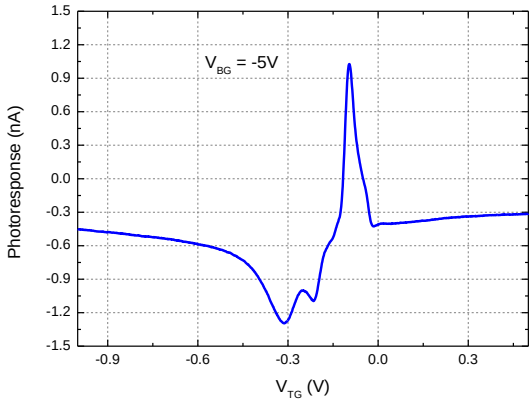
(b)



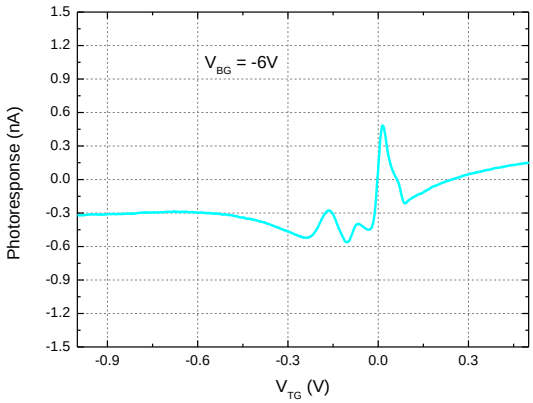
(c)


V_BG = -4V
Photoresponse (nA)
V_TG (V)

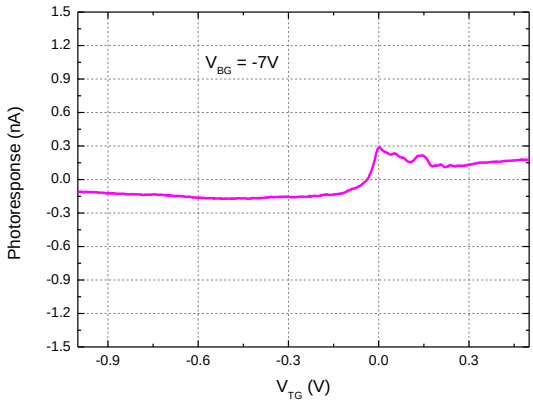
(d)


V_BG = -5V
Photoresponse (nA)
V_TG (V)

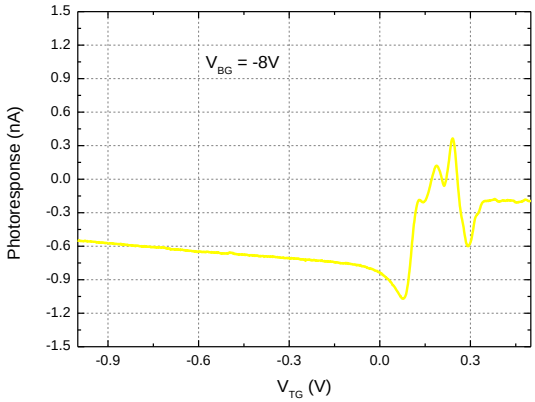
(e)


V_BG = -6V
Photoresponse (nA)
V_TG (V)

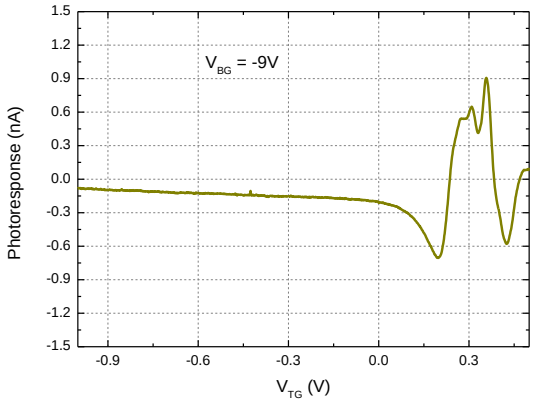
(f)


V_BG = -7V
Photoresponse (nA)
V_TG (V)

(g)


V_BG = -8V
Photoresponse (nA)
V_TG (V)

(h)


V_BG = -9V
Photoresponse (nA)
V_TG (V)

(i)

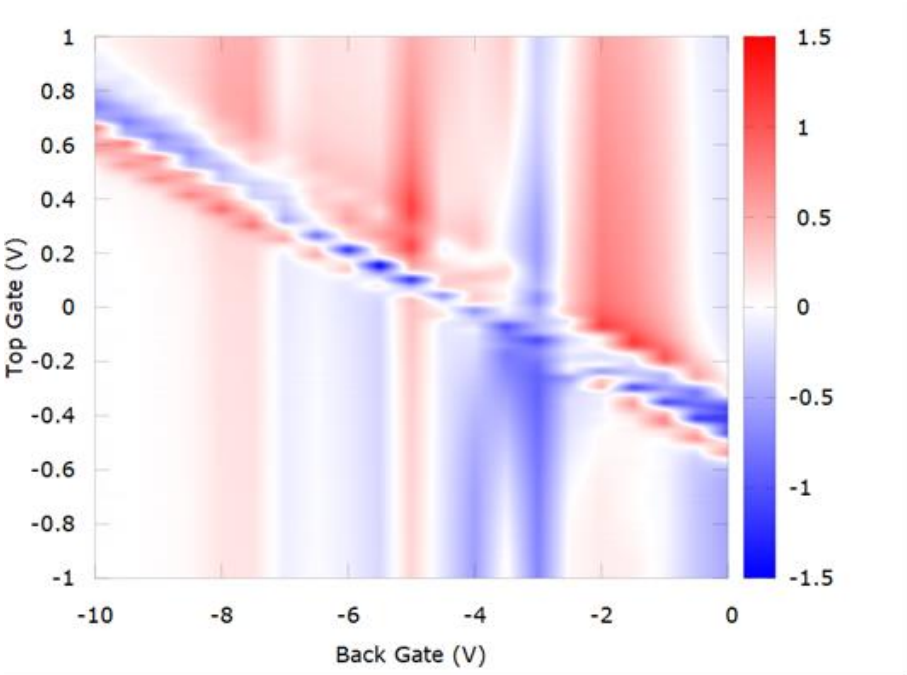


Figure 4.39 Photocurrent generated as function of the Top-Gate voltage at 4.2K and 0.3 THz when the device was polarized different back-gate voltages (a)-(h). Density map of the photocurrent generated as function of the top and back-gate voltages at 4.2K and 0.3 THz (i)

The obtained results show that the photocurrent measured vs the top gate 1 voltage is strongly influenced by the back-gate bias. This behavior is easily explained from Equation 4.1 considering that the application of a back-gate voltage modifies the overall resistance because all the three resistance contributions (R_1, R_2 and R_3) depend on the applied back-gate voltage and, consequently, the overall photocurrent curve is modified and shifted. Moreover, Figure 4.39 shows the strong dependence of the photocurrent generated with the gate voltage (Top and bottom) applied on the ADGG-GFET. Small changes on the gate voltage lead to a drop on the photocurrent generated and vice-versa.

4.5.3 4K to Troom DC and THz detection measurements

The ADGG-GFET was characterized at different temperature up to room temperature. Figure 4.40 (a) shows the CNP measurements as a function of the Back-Gate voltage for different temperatures in the 50K- 250K range.

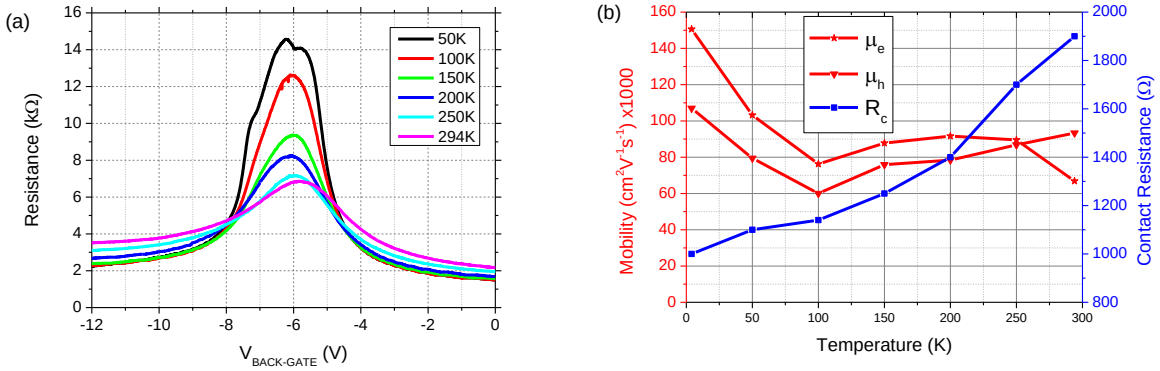


Figure 4.40 Channel resistance as function of the Back-gate voltage from 50 up to 294K (a) and the electron and hole mobilities and the channel resistance as function of the temperature (b)

At 50K, the channel resistance shows an unusual "bell" shape, similar to the one found at 4K (Figure 4.30). However, for temperatures beyond 100K the shape bercomes smoother and only one peak is observed. Moreover, the resistance at the CNP becomes lower and the electron and hole branch tails resistance raise. It is evident that the contact resistance increases when temperature increases. This increase of the contact resistance is higher for the electron branch (R=3.8kΩ at V_{BG}=-12V & T=294K) than for the hole branch (R=2kΩ at V_{BG}=0V & T=294K). By fitting the Equation (4.4) to the measured data showed in Figure 4.40 (a), the parameters μ and R_c and the dependence with the temperature can be extracted.

Figure 4.41 shows the measured photocurrent at different temperatures under excitation of 0.3 THz as a function of (a) back gate with Vg_1= Vg_2 = 0 V and (b) the boas of top gate Vg_1 with Vbg =Vg_2 = 0 V.

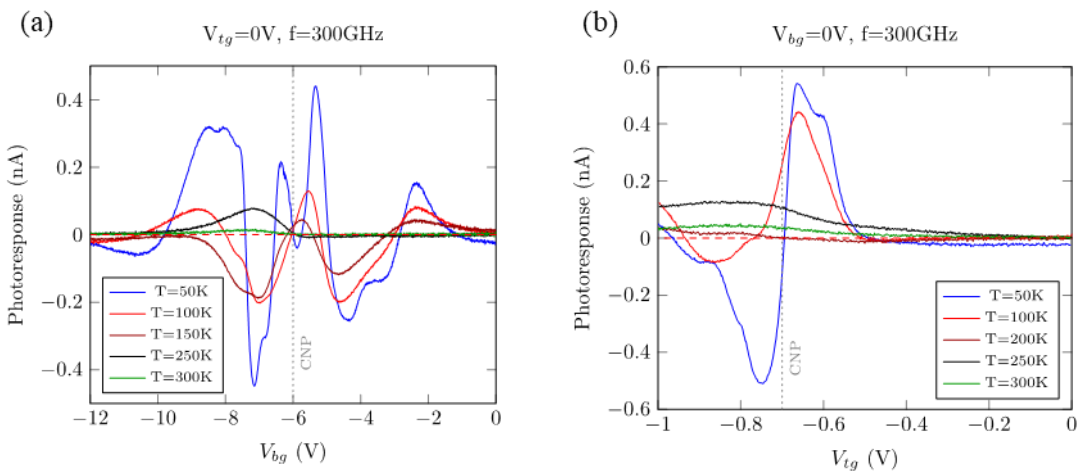


Figure 4.41 Photocurrent generated at 0.3 THz as function of the back (a) and top (b) voltages from 50 up to 300K

As the temperature is increased, the intensity of the photocurrent decreases, and some peaks vanish. At room temperature, only a small peak with an intensity of 40 pA was observed at the hole side. This can be explained as the level of the hole mobility obtained from Figure 4.40 (b) is higher than the electron mobility, enabling the detection of the THz radiation even at room temperature. ON-OFF measurements were performed on the device to analyze the performance of the device as an optoelectronic switch at different temperatures. Figure 4.42 shows the temporal photocurrent signal of the ADGG-GFET when excited at 0.3 THz (a) and the maximum photocurrent obtained as a function of the temperature (b).

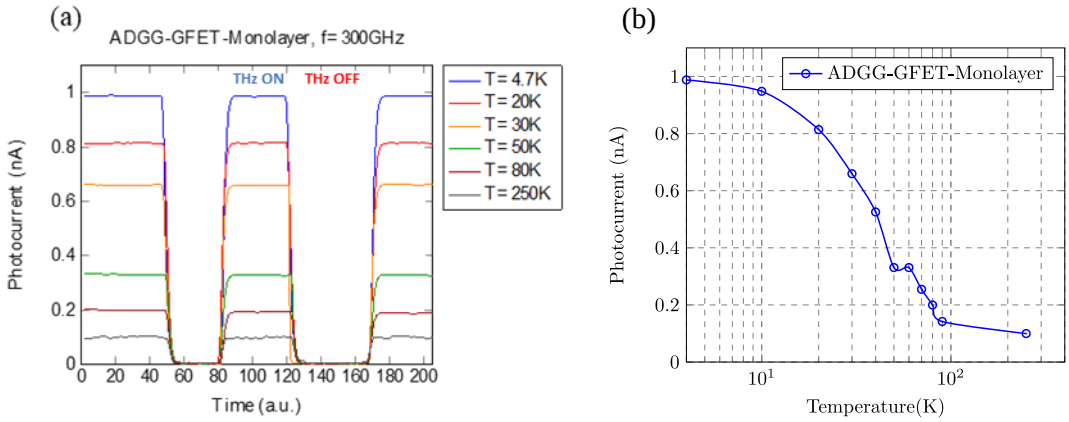


Figure 4.42 Photocurrent generated as function of the time at 0.3 THz when the THz radiation was switched ON and OFF (a) and the maximum photocurrent obtained (b) as function of the temperature

The photocurrent generated by the incoming THz radiation decreases at higher temperatures. Despite the lower level of the photocurrent generated, the photocurrent generated recovers its initial value when the THz radiation is switched ON and OFF even at high temperature. As temperature increases the photocurrent generated becomes noisier because thermal noise linearly increases with temperature. Figure 4.42 shows the temperature dependence of the maximum value of the measured photocurrent. From experimental measurements it follows that beyond 100 K the photocurrent slightly varies from 180 pA to 60 pA. Below 100K, the photocurrent generated is strongly influenced by the working temperature as the level of the photocurrent decreases from 1 nA to 0.2 nA. Obviously at the higher temperatures in the considered range, the quality factor $(\omega\tau)$ will become smaller as consequence of the lowering of the mobility. We found a quality factor value $\omega\tau \sim 0.01$ at room temperature, that is consistent with the non-resonant response found.

4.5.4 Terahertz imaging with ADGG-GFET at Room temperature

To test the ability of the ADGG-GFET as detectors in THz imaging, the device was used as sensor in the room-temperature terahertz imaging system described in Section 2.2. Figure 4.43 shows the visible image of a standard metallic surgical blade (left) and its terahertz image at 0.3 THz (right) when it was hidden inside a paper envelope. THz radiation passes through the envelope and is reflected only by the metallic parts of the surgical blade. A pixel-by-pixel image was taken using the ADGG-GFET as detector; the back-gate of the ADGG-GFET was biased to obtain a maximum value of the photocurrent generated at 0.3 THz.

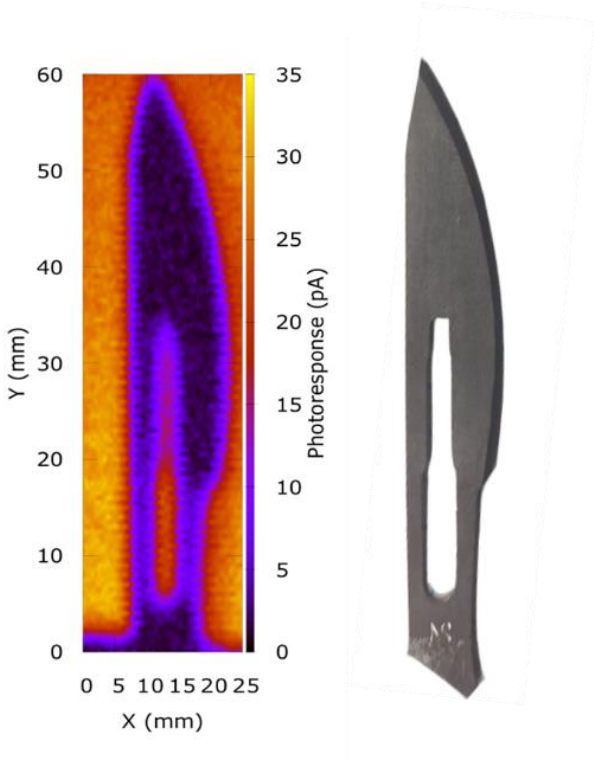


Figure 4.43 False color 0.3 THz (left) and visible (right) images of a surgical blade

The clear terahertz image of the hidden object obtained confirms the suitability of ADGG GFETs to be used as detectors to obtain high-quality THz images. Of course, better resolution could be obtained at higher frequencies.

4.5.5 Responsivity and NEP

As we mentionend in Chapter 3, Responsivity and NEP are the two main figures of merit that determine the performance of a device as THz sensor. Since the detection measurements on this chapter where performed by measuring photocurrent, small modifications must be introduced in equations (3.29) and (3.30) to calculate the current responsivity (R_I) and NEP. R_I and NEP were recalculated according to the equations 4.9 and 4.10 respectively:

$$R_I = \frac{\Delta I S_t}{P_t S_a} \frac{\pi}{\sqrt{2}} \tag{4.9}$$

$$NEP = \frac{N_{th}}{R_V} = \frac{N_{th}}{R_I \cdot R_{DS}} \tag{4.10}$$

and using as device area the diffraction limit area (S_λ (0.3 THz) ~ 0.25 mm^2) ensuring that both R_v and NEP are not overestimated s(the device area is much lower than this value).

Figure 4.44 (a) shows the Responsivity (red solid line colour) and NEP (blue solid line color) at 4K. A maximum Responsivity of 85 µA/W at 4K was found. Moreover, the minimum NEP was found close to 10^{-9} W/Hz$^{0.5}$.

(a) (b)

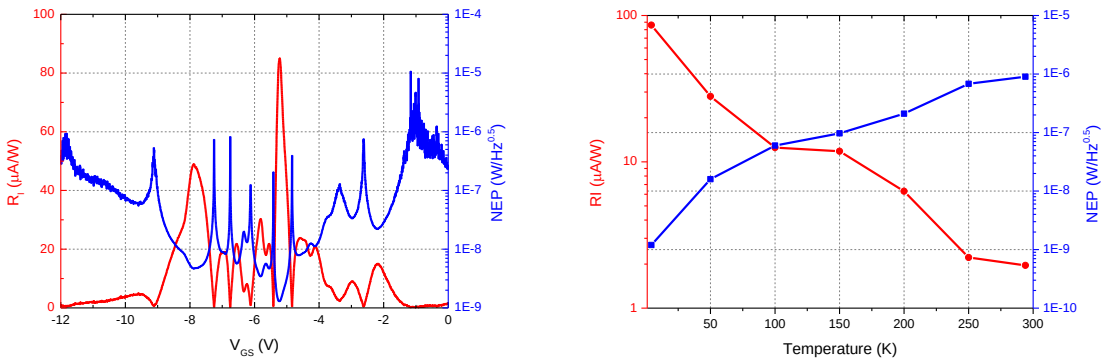


Figure 4.44 Responsivity and NEP as function of the Back-Gate voltage at 4.2K (left) and as function of the temperatura (right)

Figure 4.44 (b) shows the maximum value of the responsivity and the minimum value of the NEP as a function of the temperature. As it was showed on Figure 4.42, the highest change is found in the 4K-100K range since the responsivity decreases till a value close to 10 µA/W at 100K. At room temperature the values obtained for the Responsivity and NEP were 1.96 µA/W and 0.9 µW/Hz$^{0.5}$ respectively. We must bear in mind that these earlier values were obtained assuming a very pessimistic value of the area. Using an estimated device area of 100x100 µm^2 the values for the Responsivity and NEP are given in Figure 4.45

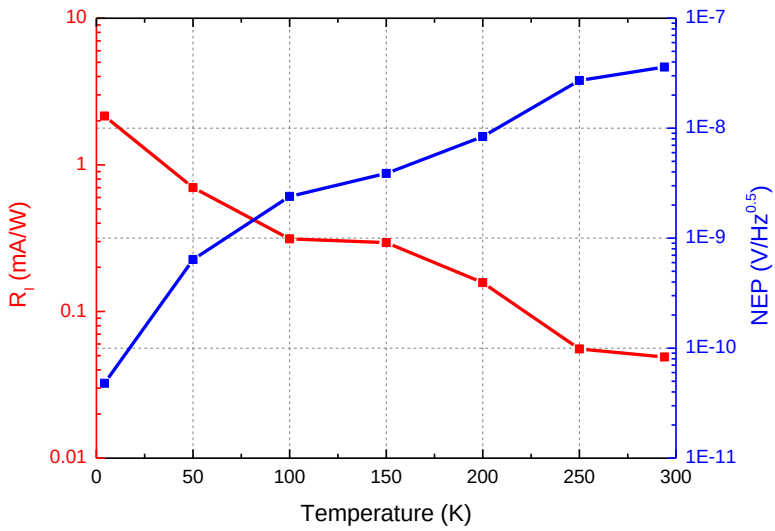


Figure 4.45 Responsivity and NEP as function of the temperatura at 0.3 THz

These values are competitive compared with previously publised results at 0.3 THz for a graphene FET on SiO_2 [92]. It should be remembered that the device studied on this thesis (ADGG-GFET) lacks of an antenna and the spot size at these frequencies is relatively big. Nevertheless, we may rightly understand that graphene encapsulation between two flakes of h-BN and the multi-gate design are responsible for the excellent performance of our device as compared to the graphene on SiO_2 transistor with a coupled antenna.

4.5.6 THz emission measurements

ADGG-GFETs are currently under investigation for THz amplification and emmiters at RIEC. The design of the ADGG-GFET includes also two asymmetric dual grating top gates. Table 4.1 summarizes the geometrical parameter of the ADGG-GFETs under studio for THz emission. Both gates have 6 fingers each with gates of different lenghts. The gates (G1 & G2) width was 15 µm to ensure the covering of the channel width (4 µm). The drain and source are made as quasi one-dimensional contacts to keep the graphene fully encapsulated and protected. The device was fabricated over a Si/SiO_2 p-doped substrate where the Silicon wafer was highly p-doped to be used as a back-gate.

	#1	#2	#3
L_1 (µm)	0.75	0.5	2
L_2 (µm)	1.5	1	2
d_1 (µm)	0.5	0.5	1
d_2 (µm)	1	2	1
S_1 (µm)	1	2	1
S_2 (µm)	0.5	0.5	1

Table 4.1 Geometrical parameters for the fabrication of the ADGG-GFETs

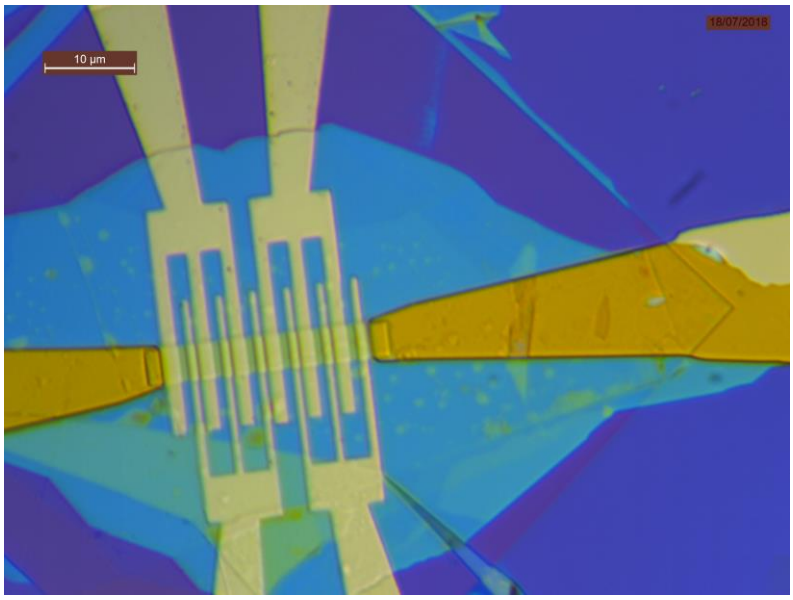


Figure 4.46 Optical image of the ADGG-GFET #2

Figure 4.20 and Figure 4.46 show the ADGG-GFETs corresponding to the desings #2 and #1 respectively (see Table 4.1). Up to now, preliminar results of the investigation cannot allow to establish if THz generation/amplification is experimentally achievable..

Summary and Future Work

The objective that is at the heart of this Thesis is the investigation of different technologies that may help the development of new reliable solid-state devices for the advancement of THz technology. To this aim, the performance of several technologies such as Si/SiGe HEMTs, FinFETs, and Graphene-based FETs to detect THz radiation was studied.

To this purpose, a THz system dedicated to both detection and imaging was mounted at the USAL TeraLab. A new cryostat that allowed THz detection at different temperatures from 4K up to room temperature was installed. All the measurements at USAL were done at two frequencies (0.15 and 0.30 THz). An external experimental setup of CEZAMAT (Warsaw, Poland) that was also used to characterize some devices in the continuous frequency range 0.14 - 0.44 THz at room temperature.

Two different silicon-based devices were proposed and studied as THz detectors. On a first stage, the experimental detection of THz radiation with strained-Si MODFETs was demonstrated. We were able to describe both the DC behavior and the THz response of the transistor using TCAD Synopsys simulator. A two-dimensional hydrodynamic-model was used in TCAD simulations to understand and predict the response of the strained-Si MODFETs. This model was validated by comparing its results with DC measurements and their first order derivatives (such as transconductance and efficiency of the transconductance). Results obtained in both experimental and simulations were in good agreement. This allowed us to subsequently use the model to obtain the response to THz radiation using the software. The agreement between simulation results and measurements was excellent. In this document, we only showed results obtained in TCAD simulations of strained-Si MODFETs as THz detectors, however, this tool can be easily extended to other materials. We studied experimentally the coupling of THz radiation with the electron channel of the FET and we found that the coupling was mainly performed by the bonding wires at 0.15 THz and by the contacts pads at 0.3 THz. THz measurements showed the great performance of these devices in terms of Responsivity and NEP (75 V/W and 0.06 nW/Hz$^{0.5}$) at room temperature.

In a second stage, an experimental work based on Silicon FinFETs as room temperature THz detectors was presented. The lack of a detailed knowledge of the internal structure of the measured FinFETs precluded us from carrying TCAD simulations of this structure. Silicon FinFETs were studied on the THz range of 0.14 up

to 0.44 THz at CEZAMAT (Warsaw, Poland) facilities. Results obtained from THz measurements show the potential of these devices as THz detectors as a consequence of the great performance obtained in terms of Responsivity and NEP. Responsivity and NEP values obtained were close to 0.7 kV/W and 0.05 nW/Hz$^{0.5}$ at 0.4 THz and at room temperature.

The other main objective of this PhD was the fabrication and characterization of Graphene-based FETs as THz detectors. Transport models for graphene are no currently implemented in TCAD, therefore the nature of our investigation on these devices was mainly experimental. A novel transfer technique and a in-house developed setup were implemented and installed in the nanotechnology Clean Room of the USAL. The newly developed transfer technique enabled the assembly of graphene layers between two flakes of h-BN. Raman measurements confirmed the quality of the graphene heterostructures fabricated and, thus, the excellent properties of graphene encapsulated on h-BN as compared to the conventional ones deposited on SiO_2. The asymmetric dual grating gate graphene FET (ADGG-GFET) concept was introduced as an efficient way to improve the response of Graphene-FETs to THz radiation. High quality ADGG-GFETs were fabricated and characterized under THz radiation. DC measurements on the ADGG-GFETs confirmed the high quality of graphene heterostructures in agreement with Raman measurements. A clear THz detection was found for both 0.15 THz and 0.3 THz at 4K when the device was voltage biased either using the back or the top gate. The measured THz response of the Graphene-FETs under excitation at 0.3 THz was found to be roughly twenty times more intense than under excitation at 0.15 THz. We also found that the photocurrent generated in the ADGG-GFET by the incoming THz could be enhanced also by biasing both top- and back-gates. Room temperature detection was achieved at 0.3 THz by using the ADGG-GFET biasing either back-gate or top-gate.

The low temperature performance of the ADGG-GFET in terms of Responsivity and NEP was 2.2 mA/W and 0.04 nW/Hz$^{0.5}$ respectively. At room temperature the values obtained for the Responsivity and NEP were 40 µA/W and 40 nW/Hz$^{0.5}$ respectively. THz imaging was performed at room temperature to test the capability of the ADGG-GFET in a real application. The transistor was successfully used as the sensor to generate a THz image a hidden object. To the best of our knowledge, this is the first experimental demonstration of an ADGG-GFET to detect EM radiation in the millimeter range (<0.3THz).

Additionally, there have been some experiments which we could not complete during this PhD. Silicon- and Graphene-based FETs were characterized in the lower range of submillimeter waves (< 0.44 THz). Experiments up to 2 THz are needed to better understand the behavior and potential of these devices to cover the THz GAP. The performance of the graphene transistor at low THz frequency (0.3 THz) was studied and a non-resonant response was found in agreement with the quality factor $\omega\tau$. Nevertheless, results obtained at low THz frequencies suggest a great potential of these devices at higher frequencies. Furthermore, the parameter $\omega\tau$ can be increased by using a THz source of a frequency higher than 0.3THz. Since the fabrication process of graphene-based heterostructures was optimized in recent runs, in the future experiments at higher frequencies will be performed looking for resonant detection of ADGG-GFETs.

Otherwise, the potential of ADGG-GFETs as THz emitters is currently explored at RIEC facilities (Tohoku University, Japan). These experiments only started recently and, after this PhD, deepen intense work will be done to obtain the potential results of ADGG-GFETs as THz emitters.

Appendix A

Resumen

FETs basados en Silicio y Grafeno para tecnología de THz

Esta tesis se enfoca al estudio de la respuesta a la radiación electromagnética de Terahercios (THz) de differentes *FETs* compatibles con substratos convencionales de silicio: *strained-Si MODFETs*, *FinFETs* y *FETs* de grafeno han sido estudiados.

La primera parte de la Tesis está dedicada a presentar los resultados de un estudio experimental y teórico de *strained-Si MODFETs*. Estos transistores fueron fabricados por epitaxia de una capa relajada de SiGe sobre un substrato convencional de Si para permitir la fabricación de un canal de Si bajo strain para obtener un gas de electrones de alta movilidad. La detección a temperatura ambiente bajo excitación de 0.15 y 0.3 THz, así como una elevada sensibilidad a la polarización de la radiación recibida han sido demostradas. Un modelo hidrodinámico en dos dimensiones fue desarrollado para realizar simulaciones de tipo TCAD para comprender y predecir la respuesta de los transistores. Los resultados experimentales y las simulaciones TCAD coinciden, validando y demostrando el potencial de TCAD como una herramienta para el diseño de futuros dispositivos de THz, así como el excelente rendimiento de los strained-Si MODFETs como detectores de THz (responsividad de 75 V/W and una potencia equivalente de ruido –NEP- de 0.06 nW/Hz$^{0.5}$). La segunda parte de la Tesis abordó el estudio experimental del comportamiento a temperatura ambiente de modernos transistores FinFETs de silicio. Los transistores FinFETs de silicio fueron caracterizados en el rango de 0.14 a 0.44 THz. Los resultados obtenidos en este estudio demuestran el elevado potencial de estos dispositivos como detectores de THz en términos de su excelente responsividad y NEP (0.66 kV/W and 0.05 nW/Hz$^{0.5}$, respectivamente).

Una gran parte de esta Tesis está dedicada a la fabricación y caracterización de FETs basados en grafeno. Una nueva técnica de transferencia y un sistema de desarrollo propio fueron implementados en la Sala Limpia de Nanotecnología de la USAL, ambos fueron descritos en detalle en la Tesis. La novedosa técnica de transferencia desarrollada permite encapsular grafeno entre dos capas de h-BN. Medidas Raman confirmaron la calidad de las heteroestructuras de grafeno fabricadas y, con ello, las excelentes propiedades del grafeno encapsulado. El concepto de FET de grafeno de puerta de rejilla doble asimétrica (ADGG-GFET) fue introducido como una forma eficiente para mejorar la respuesta a la radiación de THz de los transistores de grafeno. Dispositivos ADGG-GFET de gran calidad fueron fabricados y caracterizados bajo radiación de THz. Las medidas en DC confirmaron la gran calidad de las heteroestructuras de grafeno antes del procesado para

la fabricación del transistor en acuerdo con los resultados de las medidas Raman. Una clara detección de la señal de THz se obtuvo tanto a 0.15 como a 0.3 THz a 4K cuando el dispositivo fue polarizado en voltaje usando tanto la puerta inferior como la superior del G-FET. La detección a temperatura ambiente fue demostrada a 0.3 THz usando el ADGG-GFET. Los dispositivos mostraron a 4K una responsividad y NEP cercanos a 2.2 mA/W and 0.04 nW/Hz$^{0.5}$ respectivamente. Finalmente, se demostró el uso práctico de los dispositivos ADGG-GFET en la inspección de objetos usando un sistema de imagen de THz de desarrollo propio.

Palabras clave: THz, Ondas de Plasma, FETs, MODFETs, FinFETs, Silicio, Grafeno.

Appendix B

Conclusiones y perspectivas

El objetivo que inspira esta Tesis es la investigación de diferentes tecnologías que pueden ayudar al desarrollo de nuevos dispositivos de estado sólido para aplicaciones en el rango de THz. Para ello, se ha estudiado el rendimiento de varias tecnologías tales como Si/SiGe HEMTs, FinFETs y FETs basados en grafeno compatibles con silicio y, por lo tanto, de gran fiabilidad.

Para llevar a cabo la parte experimental de esta Tesis se instaló en el Laboratorio de Terahercios de la USAL un sistema dedicado a la medida de la detección y a la generación de imágenes en el rango de THz que usa una fuente a 0.15 y a 0.30 THz. Un nuevo criostato fue instalado para estudiar la detección de THz a diferentes temperaturas desde 4K hasta temperatura ambiente. Las medidas en la USAL se llevaron a cabo a las dos frecuencias (0.15 y 0.3 THz) mencionadas. También se utilizó un montaje experimental externo del CEZAMAT (Varsovia, Polonia) para caracterizar a temperatura ambiente algunos transistores en un rango continuo de frecuencias entre 0.14 y 0.44 THz.

Dos dispositivos diferentes basados en silicio fueron propuestos y estudiados como detectores de THz. En una primera parte, la detección experimental de radiación de THz con strained-Si MODFETs fue demostrada. Fuimos capaces de describir tanto el comportamiento en DC como la respuesta en THz de este tipo de transistor usando un simulador TCAD de Synopsys. Un modelo hidrodinámico de dos dimensiones fue utilizado en las simulaciones TCAD para entender y predecir la respuesta de los strained-Si MODFETs. El modelo fue validado comparando los resultados obtenidos en medidas DC y sus derivadas de primer orden (tales como la transconductancia y eficiencia de la transconductancia) y las simulaciones TCAD. Esto nos permitió obtener la respuesta a la radiación de THz utilizando el software TCAD y, de nuevo, la concidiencia entre la simulación y medida fue excelente. En este documento sólo mostramos los resultados obtenidos en simulaciones TCAD de la detección de señales en el rango de THz para strained-Si MODFETs, sin embargo, esta herramienta puede ser fácilmente extendida a otros materiales. Estudiamos experimentalmente el acoplamiento de la radiación de THz con el canal de electrones en estos transistores MODFET y encontramos que el acoplamiento se realizaba preferentemente mediante los hilos de bonding a 0.15 THz y mediante los contactos en el chip a 0.3 THz.

La segunda parte de la Tesis presenta un estudio experimental a temperatura ambiente de la detección de señales de THz mediante FinFETs de silicio. La asuencia de una descripción detellada de la estructura interna de los FinFETs medidos nos impidió realizar simulaciones TCAD de esta estructura. Los FinFETs fueron estudiados en el

rango de 0.14 hasta 0.44 THz en las instalaciónes de CEZAMAT (Varsovia, Polonia). Los resultados obtenidos de las medidas de muestran el gran rendimiento en términos de Responsividad y NEP. Los valores obtenidos para estas figuras de mérito fueron aproximadamente 0.7 kV/W y 0.05 nW/Hz$^{0.5}$ a 0.4 THz y temperatura ambiente.

El otro gran objetivo de esta Tesis fue la fabricación y caracterización como detectores de THz de dispositivos FET basados en grafeno. Los modelos TCAD para el transporte en grafeno no han sido todavía implementados y por ello el carácter de nuestra investigación de estos dispositivos fue principalmente experimental. Una nueva técnica de transferencia y un sistema de desarrollo propio fueron implementados e instalados en la Sala Limpia de la USAL. La novedosa técnica de transferencia permite el ensamblado de capas de grafeno entre dos copos de h-BN. Las medidas Raman confirmaron la calidad de las heteroestructuras de grafeno fabricadas y, con ello, las excelentes propiedades del grafeno encapsulado en h-BN en comparación con la técnica convencional que usa grafeno depositado sobre SiO_2. El concepto de FET con puerta de rejilla doble asimétrica (ADGG-GFET) fue introducido como una forma eficiente para mejorar la respuesta a la radiación de THz de los FET de grafeno (GFET). ADGG-GFETs de gran calidad fueron fabricados y caracterizados bajo radiación THz. Las medidas en DC confirmaron la gran calidad de las heteroestructuras de grafeno tal y como se mostró también en las medidas Raman sobre la heteroestructura antes de su procesamiento para fabricar los transistores. Una clara detección en THz fue obtenida a 0.15 y 0.3 THz a baja temperatura (4K) cuando el dispositivo fue polarizado en tensión usando tanto la puerta inferior como la superior. Se observó que la medida de la respuesta en THz del FET de grafeno bajo excitación a 0.3 THz es más de veinte veces más intensa que bajo excitación a 0.15 THz. Encontramos también que la fotocorriente generada en los ADGG-GFET por la radiación de THz podía ser mejorada también polarizando tanto la puerta superior del transistor como la inferior. La detección a temperatura ambiente utilizando el ADGG-GFET fue alcanzada a 0.3 THz tanto con polarización DC de la puerta superior como de la inferior. El ADGG-GFET mostró un rendimiento en términos de Responsividad y NEP de 2.2 mA/W and 0.04 nW/Hz$^{0.5}$ respectivamente a baja temperatura. A temperatura ambiente los valores obtenidos para la responsividad y NEP fueron de 40 µA/W and 40 nW/Hz$^{0.5}$ respectivamente. Además, se realizó una imagen de THz a temperatura ambiente para demostrar la capacidad de este dispositivo en aplicaciones reales.

Adicionalmente, debemos mencionar que ha habido algunos experimentos que no han podido completarse durante este doctorado y que se abordarán en el futuro. Los FETs basados en grafeno y silicio fueron caracterizados en el rango bajo de ondas submilimetricas (<0.44 THz). Es necesario realizar experimentos hasta 2 THz para entender el comportamiento y descubrir el potencial que tienen estos dispositivos para poder cubrir el GAP de THz. Además, aunque el transistor de grafeno fue estudiado a baja frecuencia (0.3 THz) y se obtuvo una respuesta no resonante que está de acuerdo con el factor de calidad $\omega\tau$, los resultados obtenidos sugieren un gran potencial de los GFETs a mayores frecuencias. Además de que el parámetro $\omega\tau$ se increment usando fuentes de THz de frecuencia más alta, la fabricación de heteroestructuras basadas en grafeno se ha obtimizado recientemente en la USAL, esto permitirá realizar nuevos experimentos a frecuencias superiores a 0.4THz para tratar de observar detección resonante en ADGG-GFETs.

Por otra parte, el potencial de los ADGG-GFETs como emisores de THz está empezando a ser estudiado por el RIEC (Universidad de Tohoku, Japón). Se iniciará un

intenso trabajo para investigar la emisión de THz en ADGG-GFETs una vez concluido este doctorado.

Appendix C

List of publications

- **J. A. Delgado-Notario**, V. Clericò, K. Fobelets, J. E. Velázquez-Pérez, and Y. M. Meziani, "Room-Temperature Terahertz Detection and Imaging by Using Strained-Silicon MODFETs," in *Design, Simulation and Construction of Field Effect Transistors*, InTech, 2018.

- V. Clericò, **J. A. Delgado-Notario** *et al.*, "Quantized Electron Transport Through Graphene Nanoconstrictions," *Phys. status solidi*, vol. 215, no. 19, p. 1701065, Oct. 2018.

- H. Sánchez-Martín, J. Mateos, J. A. Novoa, **J. A. Delgado-Notario**, Y. M. Meziani, S. Pérez, H. Theveneau, G. Ducournau, C. Gaquière, T. González, and I. Íñiguez-de-la-Torre, "Voltage controlled sub-THz detection with gated planar asymmetric nanochannels," *Appl. Phys. Lett.*, vol. 113, no. 4, p. 043504, Jul. 2018.

- E. Javadi, **J. A. Delgado-Notario**, N. Masoumi, M. Shahabadi, J. E. Velázquez-Pérez, and Y. M. Meziani, "Continuous Wave Terahertz Sensing Using GaN HEMTs," *Phys. status solidi*, vol. 215, no. 11, p. 1700607, Jun. 2018.

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