Nanofabrication and Characterization of High Performance Transistors Based on CVD Graphene and hBN/Graphene/hBN Heterostructure

Paolo Pedrinazzi paolo.pedrinazzi@polimi.it

Politecnico di Milano, Dipartimento di Fisica, Piazza Leonardo da Vinci 32, 20133 Milano, ITALY

Two-dimensional materials, such as graphene, MoS_2 or WSe_2 , represent a new paradigm in the thin-film transistor technology, providing also the opportunity for new device concepts. Graphene is one of the possible contenders in high-frequency electronics, mainly due to its high charge carrier mobility which exceed that of conventional high mobility semiconductors (III-V or SiGe). Scalable production techniques, such as chemical vapour deposition (CVD), can now deliver graphene on a large scale which is interesting from the industrial point of view. However, fabrication of graphene field-effect transistors (GFETs) needs further development if graphene is to compete with established semiconductor technologies. One of the main parameters degrading high-frequency response of GFETs is contact resistance, which should be reduced below 100 Ωμm to reach that of conventional high-frequency transistors. I successfully demonstrated graphene/metal contacts with a typical contact resistance below 80 Ωμm at the Dirac point. Such ultra-low contact resistance is comparable to that of InP THz transistors and provides a viable route to high-frequency GFETs. The benefits and improvements in graphene technology were tested through the fabrication and characterization of high frequency GFETs: I designed and fabricated these devices using CVD grown graphene as a channel material transferred on a 1 μm thick SiO_2 substrate, using AlO_x as a top gate dielectric. We obtained high f_{max} / f_T in GFETs, demonstrating that graphene transistor technology can compete with well-established technologies (where f_{max} and f_T are the maximum frequency of oscillation and the cutoff frequency). To further improve the frequency response of the GFETs I investigated alternative thin gate oxides, such as TiO_x, because it has very large dielectric constants. To this end, graphene inverters were realized, providing interesting results which open a path to further improvements.

One of the main limitations of graphene in technological applications is the reduction of its mobility exhibited in realistic devices. For this reason, I studied alternative substrates for GFETs which should increase mobility by suppressing the substrate induced scattering. First, I focused on STO (strontium titanate) as a high- κ substrate/gate oxide for graphene. I fabricated and characterized GFETs and graphene inverters on such substrates. Maximum transconductance around 600 μS/μm and DC voltage gain around 5 at a gate length of 2 μm were obtained, showing good electronic properties of GFETs fabricated on STO substrates. However, since mobility in these GFETs was still very low and gate leakage currents high, research on hBN (hexagonal boron nitride) was initiated. This research led to very preliminary but interesting results which need further investigations. The benefits of this material as a substrate for graphene have been widely demonstrated in literature, but not in more complex graphene devices and circuits.

Further improvements in this research field were attained with the fabrication and characterization of Van der Waals heterostructures of graphene and hBN. I developed my

own procedure capable of realizing hBN/graphene/hBN heterostructures in which the thickness of the top hBN layer was below 8 nm, preserving at the same time the improvement of the electrical properties provided by such encapsulation. Both Raman and electrical characterizations were performed on these devices, first for a pre-selection of the high-quality areas for the fabrication of final devices and second to link the optical and electronic properties as a test of the technological improvements. The heterostructures were electrically characterized, from room to cryogenic temperatures (4 K). I obtained a large quantity (and quality) of doping-homogeneous stacks (doping concentration $<10^{12}$ cm^{-2}) with large mobility of graphene (between 25000 and 50000 cm^2 V^{-1} s^{-1} at room temperature), which were measured by the Van der Pauw method. This reflects the method optimizations I performed, leading to a more stable technology (for the graphene encapsulation) and to more scalable fabrication. We also demonstrated that it is not possible to use thin hBN as a thin top gate insulator at room temperature due to high leakage currents through such low number of hBN layers. From a technological point of view, these first studies are quite important because the implementation of thin hBN as a top gate insulator is one of the main goals of the state-of-the-art graphene electronics.

The presented studies open path to new research projects. From a “graphene electronics” point of view, the purpose is to increase performances of already demonstrated devices by replacing CVD graphene (channel material) with high-mobility encapsulated graphene and using hBN as a top gate insulator (with some additions to prevent leakage currents). This also implies other studies, for example of contact resistance, which is now incompatible with the requirements for high frequency transistor operation. Finally, these studies should allow better understanding of required improvements of graphene high-frequency devices, both from a technological and fundamental point of view.

Más información: Enrique Diez –enrisa@usal.es

Días: **martes 27 de junio de 2017**
Hora: **16:30 horas**
Lugar:

Aula 11.2 – 1ª planta –
Edificio I+D+i de la Universidad de Salamanca.
C/ Espejo, s/n. 37008 Salamanca